SECTION IX L
ASCII INTERFACE
5312A

OPERATING AND SERVICE MANUAL

SERIAL PREFIX: 1428A, 1436A

This section applies directly to HP Model 5312A ASCII Interface having serial number prefix 1428A or 1436A. Insert this document into the 5300B Measuring System manual.

Printed: SEP 1975

MANUAL PART NO. 05312-90004
MICROFICHE PART NO. 05312-90005

PRINTED IN U.S.A.

HEWLETT hp PACKARD

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF TABLES

LIST OF FIGURES

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION I
GENERAL INFORMATION

9L-1-1. PURPOSE AND USE OF SECTION IX L

9L-1-2. Section IX L contains the documentation necessary to install and operate the Hewlett-Packard Model 5312A ASCII (HP-IB) Interface. This information is intended to be inserted into the 5300B Measuring System manual as part of Section IX of that manual.

9L-1-3. DESCRIPTION

9L-1-4. The 5312A is a plug-between module for the HP 5300B Measuring System. The 5312A plugs between the 5300B mainframe and any associated plug-on module (5301A-5308A) to provide an interface to the Hewlett-Packard Interface Bus. The 5312A can provide measurement data from the 5300B via the bus to compatible printers, desk top calculators, or computers. The measurement data includes all significant digits, exponent, overflow, and function codes. Specifications for the 5312A are listed in Table 9L-1-1.

9L-1-5. INSTRUCTION IDENTIFICATION

9L-1-6. Hewlett-Packard uses a two-section, nine-digit serial number (0000A00000) mounted on the rear panel to identify the instrument. The first four digits are the serial prefix and the last five digits refer to the specific instrument. If the serial prefix on your instrument differs from that listed on the title page of this section, there are differences between the manual and your instrument.

9L-1-7. MANUAL CHANGES

9L-1-8. The title page lists the serial prefix numbers to which this information directly applies. If the serial prefix is different from the one listed, a change sheet is included describing the required changes. If this change sheet is missing, the information can be supplied by any Hewlett-Packard Sales and Service Office listed in Section VI of the 5300B Measuring System Manual.

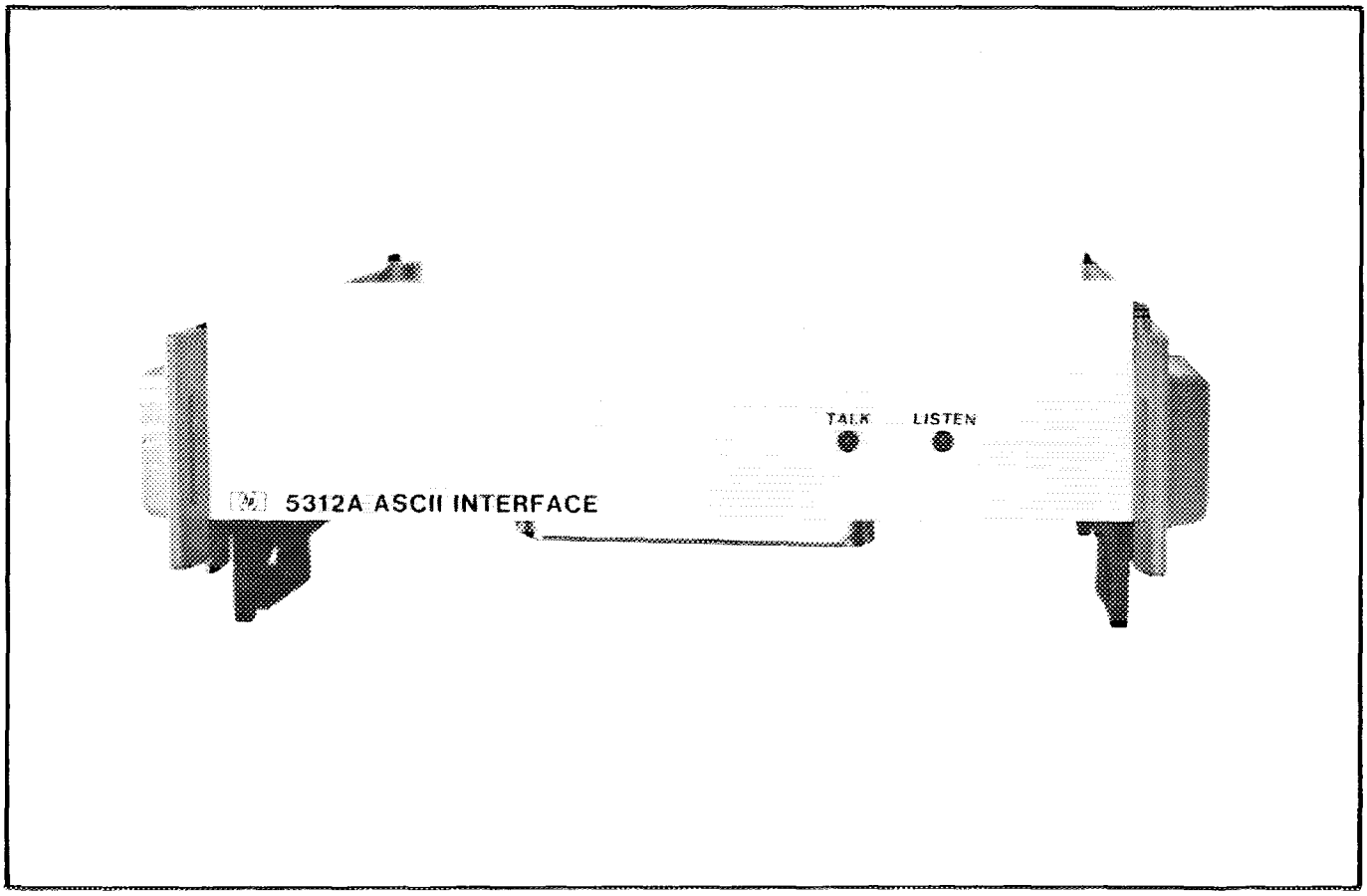


Figure 9L-1-1. 5312A ASCII (HP-IB) Interface

Table 9L-1-1. Specifications

SAMPLE RATE:
Controlled by setting of SAMPLE RATE control on front panel of 5300B mainframe or by Initiate command on interface bus.

TRANSFER TIME:
20 ms (typical) per measurement.

TRANSFER RATE:
Maximum of 40 measurements per second (depending on capabilities of plug-on module and controller).

SELF CHECK:
Rear panel switch setting provides self test of internal circuits (refer to paragraph 9L-3-32) and also activates internal test points for use with external test equipment.

INDICATORS:
TALK indicator illuminates when addressed to talk. LISTEN indicator illuminates when addressed to listen.

PROGRAMMABILITY:
Front panel controls of plug-on modules (5301A-5308A) are not programmable.

COMPATIBILITY:
Compatible with 5300B mainframe and all plug-on modules (5301A-5308A). Not compatible with 5300A which has a BCD digital output.

DIMENSIONS:
5312A plugs-between 5300B mainframe and plug-on module. Increases height of instrument by 1.5 in. (38,4 kg).

NET WEIGHT:
1 lb. 13 oz. (0,818 kg).

SHIPPING WEIGHT:
2 lbs. 10 oz. (1,19 kg).

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION II
INSTALLATION

9L-2-1. UNPACKING AND INSPECTION

9L-2-2. If the shipping carton is damaged, ask that the carrier's agent be present when the instrument is unpacked. Inspect the instrument for damage, such as scratches, dents, broken knobs, etc. If the instrument is damaged or fails to meet performance tests when used with the 5300B Measuring System, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. Sales and Service Offices are listed at the back of the 5300B portion of the manual. Retain the shipping carton and the padding material for the carrier's inspection. The Sales and Service Office will arrange for the repair or replacement of the instrument without waiting for the claim against the carrier to be settled.

9L-2-3. STORAGE AND SHIPMENT

9L-2-4. PACKAGING. To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Your Hewlett-Packard Sales and Service Office can provide packaging material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice. The instrument is originally packaged as follows: The original container is a corrugated cardboard box with 200 lbs. burst test (HP No. 9211-1760). The instrument is secured and protected in the box by a top and bottom molded frame of polystyrene foam (HP No. 9220-1545). Also included with the instrument are plastic dust covers (HP No. 9220-1762).

9L-2-5. ENVIRONMENT. Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 25,000 ft.

b. Minimum temperature: -40°F (-40°C).

c. Maximum temperature: +167°F (+75°C).

9L-2-6. INSTALLATION AND REMOVAL

9L-2-7. The 5312A must be used with a 5300B mainframe and plug-on that will make the desired measurement. Separate the 5300B mainframe from the plug-on, install the 5312A and reinstall the mainframe according to the following procedure (refer to Figure 9L-2-1):

a. Turn ac power off and disconnect power cord.

b. Pull the two side casting latches on the 5300B mainframe fully rearward while pressing the latch handles toward the outside of the casting.

c. When the latches are fully rearward, the two instrument castings will be separated about ⅛-inch.

d. Lift the 5300B mainframe gently away from the plug-on.

e. Place the 5312A on top of the plug-on and position the two units carefully so the 5312A casting aligns with the plug-on casting and approximately ⅛-inch clearance exists between the two castings.

f. Place the 5300B mainframe on top of the 5312A and mate the two units together in the same manner as described in step "e" above.

g. Push the 5312A latch handles inward until the castings come together and the latches lock in place.

h. To remove the 5312A, reverse the above procedure.

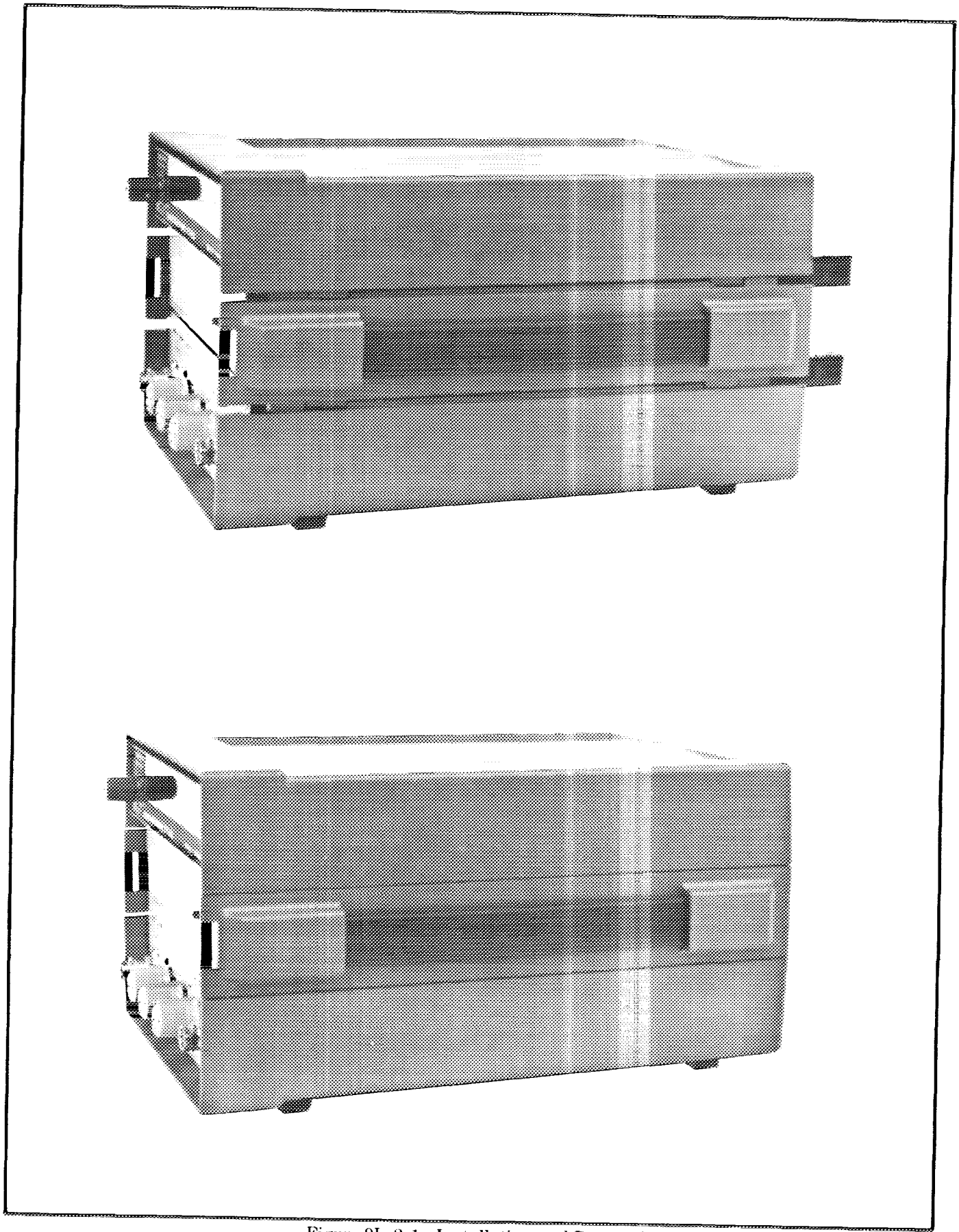


Figure 9L-2-1. Installation and Removal

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION III
OPERATION

9L-3-1. INTRODUCTION

9L-3-2. This section contains operating information including a description of controls and indicators, types of operation, triggering function, operating procedures, a system example, and self-check procedures.

NOTE

For general information on HP Interface Bus operation refer to the manual entitled "Condensed Description of the Hewlett-Packard Interface Bus, HP Part No. 59401-90030."

9L-3-3. CONTROLS AND INDICATORS

9L-3-4. Figure 9L-3-1 identifies and describes the front and rear panel controls and indicators.

9L-3-5. TYPES OF OPERATION

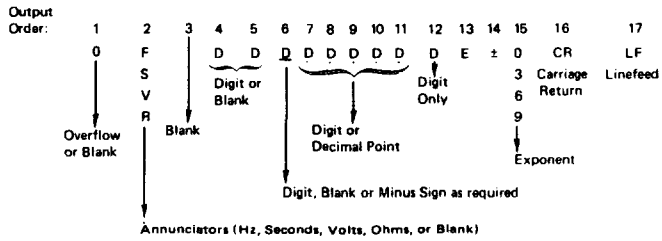
9L-3-6. The 5312A operates as an interface plug between for the 5300B Measuring System and HP Interface Bus. The 5312A can be triggered by a talker or can be set to automatically provide continuous measurement data from the 5300B to the bus. The 5312A operates with all plug-on modules (5301A-5308A) in all modes of operation except the totalize modes of the 5301A, 5302A, and 5304A. Remote triggering information is provided in the following paragraphs.

9L-3-7. INITIATE FUNCTION

9L-3-8. The 5312A is triggered via the bus to send a reset pulse to the 5300B that initiates a measurement. This action occurs when a talker sends an Initiate command (ASCII "I") to trigger the 5312A or when a controller sends a Group Execute Trigger (ASCII backspace "BS") to trigger several types of instruments. The measurement data is held by the 5312A until it is addressed to talk and send data on the bus. The talk output format is described in paragraph 9L-3-9.

9L-3-9. Talk Output Format

9L-3-10. When the 5312A is addressed to talk it provides a digital output to the interface bus. The output consists of 17 ASCII coded characters in the following format.



9L-3-11. Addressing

9L-3-12. Before a 5312A can accept an Initiate command it must be addressed to listen and before the 5312A can output data it must be addressed to talk if the rear panel switch is in the ADDRESSABLE position. When this switch is in the TALK ONLY position the 5312A automatically outputs measurements continuously without being addressed. The TALK ONLY position is intended for operation where there is no controller, e.g., with a printer. To meet bus requirements, the SHIELD switch on the rear panel should be in SHIELD position only when the TALK ONLY ADDRESSABLE switch in the TALK ONLY position.

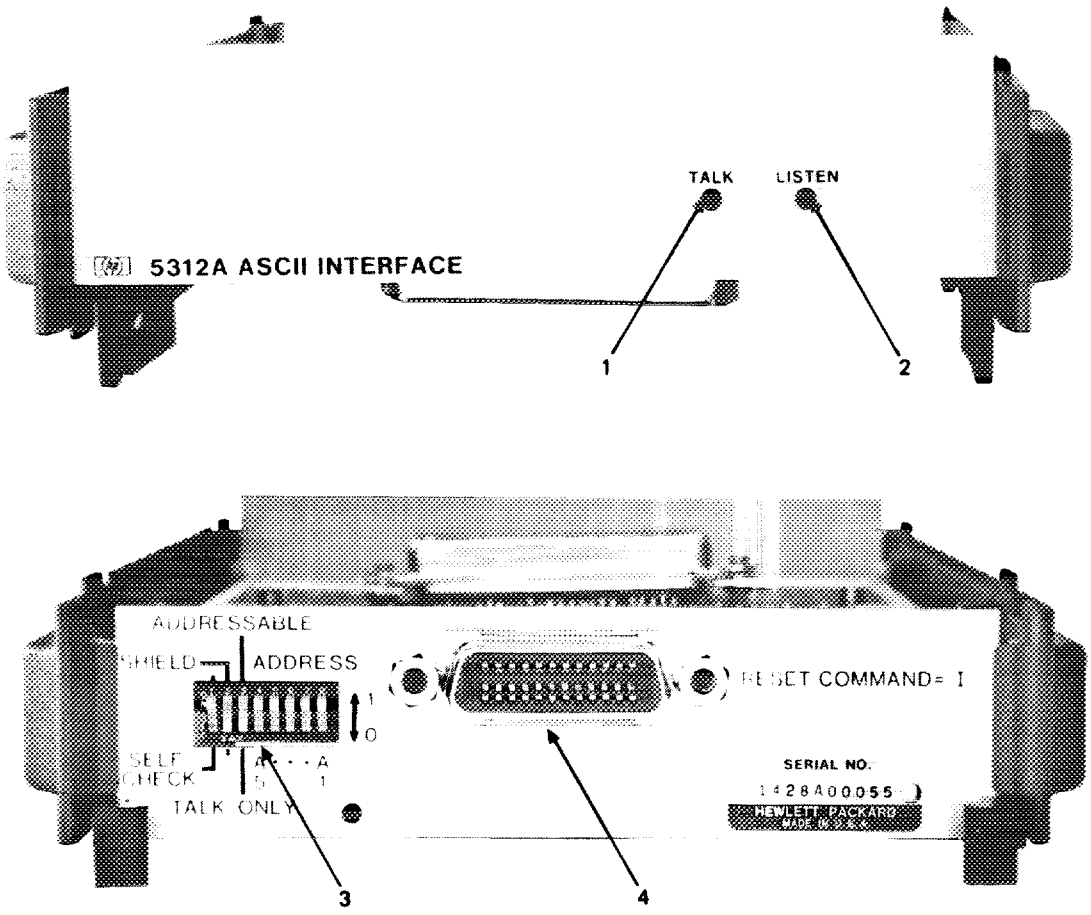
9L-3-13. The address characters sent on the interface bus must coincide with the settings of the ADDRESS switches (A1-A5) on the rear panel of the 5312A (see Table 9L-3-1). Addresses are sent on the data input/output (DIO) lines. When the controller sets ATN low, all instruments on the bus may interpret the information on lines DIO1 to DIO5 as an address. During this time, the logic level (1 or 0) on DIO6 and DIO7 designate whether the information is a talk or a listen address or a command.

9L-3-14. Unaddressing

9L-3-15. Two characters are reserved for the special function of clearing or removing an instrument from the active state of an addressed talker or listener. The 5312A is cleared as a listener if it is sent an ASCII "?" while ATN is low. The 5312A is cleared as a talker if another instrument is addressed to talk or it is sent an ASCII "_" (underscore) while ATN is low. It is cleared as either a talker or listener when IFC is low.

NOTE

When an instrument is addressed from a listener to a talker or talker to a listener, the appropriate clear codes ("?" or "_") must be issued. If underscore is not available, address a nonexistent talker.



1. TALK indicator. When illuminated, indicates the 5312A is addressed to talk.

2. LISTEN indicator. When illuminated, indicates the 5312A is address to listen.

3. Control switch. This switch controls the operation of the 5312A as follows:

   a. ADDRESS. The settings of A1-A5 determine the listen or talk address of the 5312A. Refer to Table 9L-3-1.

   b. ADDRESSABLE-TALK ONLY. When this switch is in the ADDRESSABLE position, the 5312A will not listen or talk unless addressed to do so. When this switch is in the TALK ONLY position, the 5312A outputs continuously without being addressed.

   c. SHIELD. This switch must be in the SHIELD position when the ADDRESSABLE-TALK ONLY switch is in the TALK ONLY position. (This meets the the bus requirement that the controller must connect the bus cable shield to common.)

   d. SELF CHECK. When this switch is in the SELF CHECK position the 5312A can perform a self test (see paragraph 9L-3-32).

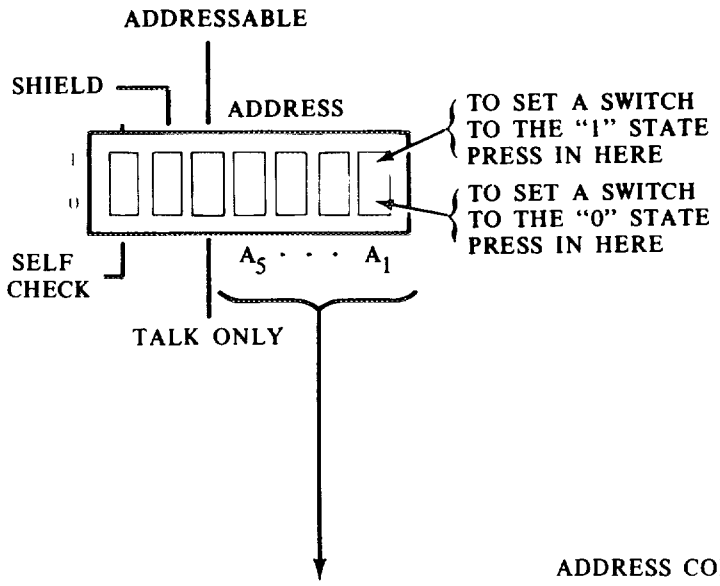
4. Connector. This 24-pin connector connects to the HP Interface Bus cable (Part No. 10631A, B, or C).

NOTE

On later models of the 5312A the top position of the SELF CHECK switch is marked NORM to indicate normal operation and the label "RESET COMMAND = I" is changed to "INITIATE COMMAND = I".

Figure 9L-3-1. Controls and Indicators

Table 9L-3-1. Address Switch Settings



SWITCH SETTINGS					ADDRESS CODES	
A_5	A_4	A_3	A_2	A_1	ASCII LISTEN ADDRESS	ASCII TALK ADDRESS
0	0	0	0	0	SP	@
0	0	0	0	1	!	A
0	0	0	1	0	"	B
0	0	0	1	1	#	C
0	0	1	0	0	$	D
0	0	1	0	1	%	E
0	0	1	1	0	&	F
0	0	1	1	1	'	G
0	1	0	0	0	(	H
0	1	0	0	1	)	I
0	1	0	1	0	*	J
0	1	0	1	1	+	K
0	1	1	0	0	,	L
0	1	1	0	1	-	M
0	1	1	1	0	.	N
0	1	1	1	1	/	O
1	0	0	0	0	0	P
1	0	0	0	1	1	Q
1	0	0	1	0	2	R
1	0	0	1	1	3	S
1	0	1	0	0	4	T
1	0	1	0	1	5	U
1	0	1	1	0	6	V
1	0	1	1	1	7	W
1	1	0	0	0	8	X
1	1	0	0	1	9	Y
1	1	0	1	0	:	Z
1	1	0	1	1	;	[
1	1	1	0	0	<	\
1	1	1	0	1	=	]
1	1	1	1	0	>	^

9L-3-16. OPERATING PROCEDURES

9L-3-17. Operating procedures consist of preliminary set-up procedures, programming procedures, and programming codes.

9L-3-18. Preliminary Set-Up Procedures

9L-3-19. The following procedures are used to place the 5312A into operation.

a. Install the 5312A between the 5300B mainframe and the plug-on module that will be used to make the measurements. Refer to Subsection II for installation information.

b. Set the mode switch (Figure 9L-3-1) to the ADDRESSABLE mode or the TALK ONLY mode as described below:

1. ADDRESSABLE mode. In this mode the 5312A must be addressed to listen before it will accept an Initiate command and must be addressed to talk before it will output. This mode is used in systems with a controller capable of addressing instruments.

2. TALK ONLY mode. In this mode the 5312A outputs continuously without being addressed. This mode is used in a system without a controller where measurement data from 5300B is sent via the 5312A to a listening device such as a printer.

c. If the mode switch is set to the ADDRESSABLE mode, select a listen address from Table 9L-3-1 and set the address switches on the rear panel of the 5312A. In general, any address switch setting is allowable except 11111 or an address already assigned to another instrument in the system. These switches need not be set if the mode switch is in the TALK ONLY mode.

d. Connect the 5312A into the system by connecting the HP Interface Bus interconnect cable from any other 24-pin bus connector in the system to the 24-pin bus connector on the rear panel of the 5312A. The 5312A is now ready for programming. Procedures are described in paragraph 9L-3-22 and codes are listed in Table 9L-3-2.

9L-3-20. Programming Codes

9L-3-21. A description of the codes used in programming the 5312A is summarized in Table 9L-3-2.

NOTE

When the 5312A is used with the 5150A Thermal Printer equipped with Option 003, the PRT CMD switch on the 5150A HP-IB Interface board must be in the LF position.

9L-3-22. Programming Procedures

9L-3-23. Perform the following steps to operate the 5312A when triggering by a controller (for nontriggered operation refer to paragraph 9L-3-25):

NOTE

If the 5312A is to be triggered simultaneously with *other types* of instruments on the bus, proceed to paragraph 9L-3-24.

a. Using a controller such as a 9820A/9830A Calculator, send the Unlisten command. This command is the ASCII question mark character "?" (with ATN low). Refer to Table 9L-3-2.

b. Send the talk address of the controller.

c. Send the listen address of the 5312A. Refer to paragraph 9L-3-19c.

NOTE

In the following step, the controller acts as a talker.

d. Send the Initiate command, ASCII "I".

NOTE

The 5312A has now been triggered to reset the 5300B mainframe. The 5312A will hold the next measurement taken until addressed to talk and send data on the bus.

e. Send the Unlisten command.

f. Send the talk address that corresponds to the address switch settings of the 5312A. Refer to Table 9L-3-1.

g. Send the listen address of any instrument on the bus that is to receive the output of the 5312A.

Table 9L-3-2. Programming Codes

Signal/Code	DIO LINES 7654321	Remarks	5312A Response
Listen Address Codes	Refer to Table 9L-3-1	Any ASCII code of the form 0 1 A_5 A_4 A_3 A_2 A_1 where $A_5 \rightarrow A_1$ can be any combination of 1's and 0's except 11111.	Illuminates LISTEN indicator. Prepares 5312A to accept the Initiate Command.
Talk Address Codes	Refer to Table 9L-3-1	Any ASCII code of the form 1 0 A_5 A_4 A_3 A_2 A_1 where $A_5 \rightarrow A_1$ can be any combination of 1's and 0's except 11111.	Illuminates TALK indicator. Causes 5312A to output on the bus.
Initiate Command	1001001	ASCII "I"	Causes 5312A to send a reset pulse to the 5300B to take a measurement.
Group Execute Trigger	0001000	ASCII "BS"	Causes 5312A to send a reset pulse to the 5300B to take a measurement.
Unlisten Command	0111111	ASCII question mark "?" character unaddresses all listeners.	Extinguishes LISTEN indicator and clears the 5312A as a listener.
Untalk Command	1011111	ASCII underscore "_" character unaddresses all talkers.	Extinguishes TALK indicator and clears the 5312A as a talker.
Interface Clear (IFC)	NA	The controller sets the IFC line low to halt all activity on the bus.	Extinguishes LISTEN and TALK indicators. Unaddresses 5312A.

NOTE

The ASCII commands Group Execute Trigger (GET), Unlisten and Untalk are Universal Address Commands (effective when ATN is low).

9L-3-24. To trigger the 5312A and *other types* of instruments simultaneously, proceed as follows:

a. Using a controller such as a 9820A/9830A Calculator, send the Unlisten command. This command is the ASCII question mark character "?" (with ATN low). Refer to Table 9L-3-2.

b. Send the listen address of each instrument to be triggered.

c. Send the universal addressed command Group Execute Trigger (GET). This command is the ASCII backspace character "BS" (with ATN low).

NOTE

All instruments addressed to listen and designed to respond to the GET command will now be triggered. The 5312A will hold the next measurement taken until addressed to talk on the bus.

d, To address the 5312A to talk, perform steps e, f, and g of paragraph 9L-3-23.

9L-3-25. To operate the 5312A in the nontriggered ADDRESSABLE mode proceed as follows (refer to paragraph 9L-3-19 for preliminary set-up):

a. Set the mode switch (Figure 9L-3-1) to ADDRESSABLE.

b. Using a controller, send the Unlisten command. Refer to Table 9L-3-2.

c. Send the talk address of the 5312A.

d. Send the listen address of the listener.

e. Adjust the SAMPLE RATE control on the 5300B mainframe to control the rate of the 5312A output data.

9L-3-26. To operate the 5312A in the TALK ONLY mode proceed as follows (refer to paragraph 9L-3-19 for preliminary set-up):

a. Set the mode switch (Figure 9L-3-1) to TALK ONLY.

b. Set the listener to the LISTEN ONLY mode.

c. Adjust the SAMPLE RATE control on the 5300B mainframe to control the rate of the 5312A output data.

9L-3-27. SYSTEM EXAMPLE

9L-3-28. An example of the use of the 5312A and the 5300B in a data acquisition system would include a 5306A Multimeter/Counter plug-on module and a 9820A/9821A Calculator. The calculator acts as a controller and is connected to the 5312A via the HP Interface Bus interconnect cable. The calculator can be programmed to acquire, store, and manipulate the measurement data by means of brief program statements. For example, assume that the 5312A address switches are set for a talk address of J and the calculator has a listen address of 5. The program statement to read a measurement into the Z register of the calculator would be:

CMD "?J5";FMT *; RED 13,Z

The above statements are defined as follows:

CMD	Bus command statement. Refer to 11224A Peripheral Control II operating manual (HP Part No. 09820-90024) for complete description.
"	First quotes following CMD statement specifies address mode.
?	Unaddresses all listeners on the bus.
J	5312A talk address.
5	Calculator listen address.
"	Terminates address mode.
;	End-of-statement delimiter.
FMT*	Free-field format.
;	End-of-statement delimiter.
RED 13,Z	Read data on the bus through the calculator interface card to the Z register in the calculator.

9L-3-29. To add overflow and annunciator information to the above format, execute the following:

CMD "?J5";RDB 13→A; RDB 13→B; FMT*; RED 13,Z

After execution of these statements the A register of the calculator would contain the decimal equivalent of the first ASCII character output by the 5312A (79 for overflow or 32 for space). The B register would contain the decimal equivalent of the second character output by the 5312A (70 for frequency, 83 for seconds, 86 for volts, 82 for ohms, and 32 for space). Refer to 11224A Peripheral Control II operating manual (HP Part No. 09820-90024) Table 2-1.

9L-3-30. In the preceding examples, the 5312A outputs measurement data at a rate controlled by the setting of the SAMPLE RATE control on the 5300B mainframe. The calculator may take control and command measurements to be taken by executing the following statement (the address switch setting which gives the 5312A a talk address of J also gives it a listen address of * and the calculator has a talk address of U):

CMD "?U*", "I"

The Initiate (I) command in this statement causes the 5312A to reset the 5300B to take a measurement. The 5312A then holds the measurement data until it is addressed to talk. Refer to paragraph 9L-3-23.

9L-3-31. After the measurement data is entered into the calculator, a wide variety of useful tasks may be performed, from sorting and storing of data to complex statistical analyses.

9L-3-32. SELF CHECK PROCEDURES

9L-3-33. The self check of the 5312A checks the circuits as described in paragraph 9L-5-21 and as shown in Figure 9L-8-2 (Sheet 3). Perform the self check as follows:

a. Install the 5312A as described in paragraph 9L-2-6 and apply power.

b. Disconnect the HP-IB cable from the 5312A.

c. Set the switches on the rear panel of the 5312A to the following positions:

1. Press all address switches (A1-A5) to 0 (bottom pressed in).
2. Press the TALK ONLY/ADDRESSABLE switch to ADDRESSABLE position.
3. SHIELD switch in either position.
4. Reset the 5312A by turning the power off (on 5300B) then back on.
5. Press SELF CHECK switch to SELF CHECK position.

NOTE

The self check will not operate properly unless the right-most digit on the display is a zero.

d. Correct operation of the 5312A is indicated as follows:

   1. The 5300B display is illuminated with an 8 in each digit position, decimals in the 5 right-most positions and overflow.

   2. The TALK indicator on the 5312A is illuminated.

   3. If indications are correct, turn off power, set SELF CHECK switch to normal, and turn power back on.

   4. If indications are incorrect (5300B display cycles from all 0's through all 9's), refer to the self check trouble isolation procedure described in paragraph in 9L-5-21.

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION IV
THEORY OF OPERATION

9L-4-1. INTRODUCTION

9L-4-2. This section contains theory of operation including an *overall functional* description to the block level, a *detailed* description to the *block level* and a *detailed circuit* description to the schematic diagram level. An operational flowchart description of software program operation is also included. For a description of HP Interface Bus operation, refer to the manual entitled Condensed Description of the Hewlett-Packard Interface Bus, HP Part No. 59401-90030.

9L-4-3. OVERALL FUNCTIONAL DESCRIPTION

9L-4-4. The 5312A ASCII Interface plugs between the 5300B mainframe and any associated plug-on module (5301A-5308A) to provide an interface to the HP Interface Bus (HP-IB). The 5312A provides measurement data from the 5300B to the HP-IB including all significant digits, exponent, overflow, and function codes.

9L-4-5. As shown in Figure 9L-4-1, the operation of the 5312A is controlled by an Algorithmic State Machine (ASM) control circuit which has a number of inputs and outputs. The ASM contains a preprogrammed Read-Only-Memory (ROM) which selects an input (called a qualifier) from one of several lines from the 5300B, the HP-IB, or the 5312A circuit. The ASM controls output data to the HP-IB via a multiplexer circuit and sends commands to the 5300B and to the internal circuit. The ASM control circuit determines whether the data from the 5300B or the control circuit is sent to the HP-IB. Note that the three-most-significant bits of the output character are always sent from the ASM. This arrangement allows the ASM to control the output as described in the detailed description that follows.

9L-4-6. DETAILED BLOCK DIAGRAM DESCRIPTION

9L-4-7. The 5312A operates basically as a synchronous device controlled by preprogrammed instructions. The instructions are programmed into a 4K Read-Only-Memory (ROM) as the control element of an Algorithmic State Machine (ASM). As shown in Figure 9L-4-2, the measurement data from the 5300B mainframe is processed by the 5312A and supplied as ASCII coded characters to the HP Interface Bus. The following programs describe the circuits shown in the detailed block diagram.

9L-4-8. The Address Logic circuit monitors the bus Data Input/Output (DIO1-DIO7) lines to detect a listen or talk address. The circuit then sets the 5312A in the listen or talk mode of operation and sends a qualifier to the ASM control circuit qualifier multiplexer. The DIO lines are also monitored for a trigger command from a controller. The trigger command is supplied to the ASM control circuit as a qualifier to the ASM which in turn causes a measurement to be taken by the 5300B.

9L-4-9. The Algorithmic State Machine (ASM) controlled by a programmed 4K ROM selects input qualifiers by means of a multiplexer and Qualifier Control circuit. The inputs come from the 5300B mainframe, from the interface bus, and from internal registers. The Qualifier Control circuit is enabled by an instruction from the ROM. The Qualifier Control circuit outputs a signal that causes a jump in the program sequence. When not enabled it allows the program to proceed in numerical sequence to the next program line number (addresses). The ASM also provides output instructions to the Output Logic and Data Multiplexer circuits.

9L-4-10. The State Counters are incremented by one at each clock pulse to allow the ROM program to proceed from one address line to the next in sequence. When the Preset Enable line of the State Counters is enabled, the State Counters are loaded with the link address from the ROM. The ASM will jump to this link address if the selected qualifier is in the correct state.

9L-4-11. The Output Logic circuit processes instructions from the ROM and provides output data and a latch clock to the Data Multiplexers. The Reset and Hold signal lines connect to the mainframe and a Talk/Listen clock goes to the Address Logic to enable the Talk and Listen FFs. The Output Logic also provides an Increment signal to the Position Counters. The Output Logic is enabled by the $\overline{\text{CLK}}$ signal from the Circuit Clock.

9L-4-12. The Data Multiplexers receive data from the Output Logic and from the 5300B mainframe. The selection of data is controlled by the ROM program to provide the proper talk output format to the HP-IB via the Latches/Buffers circuits.

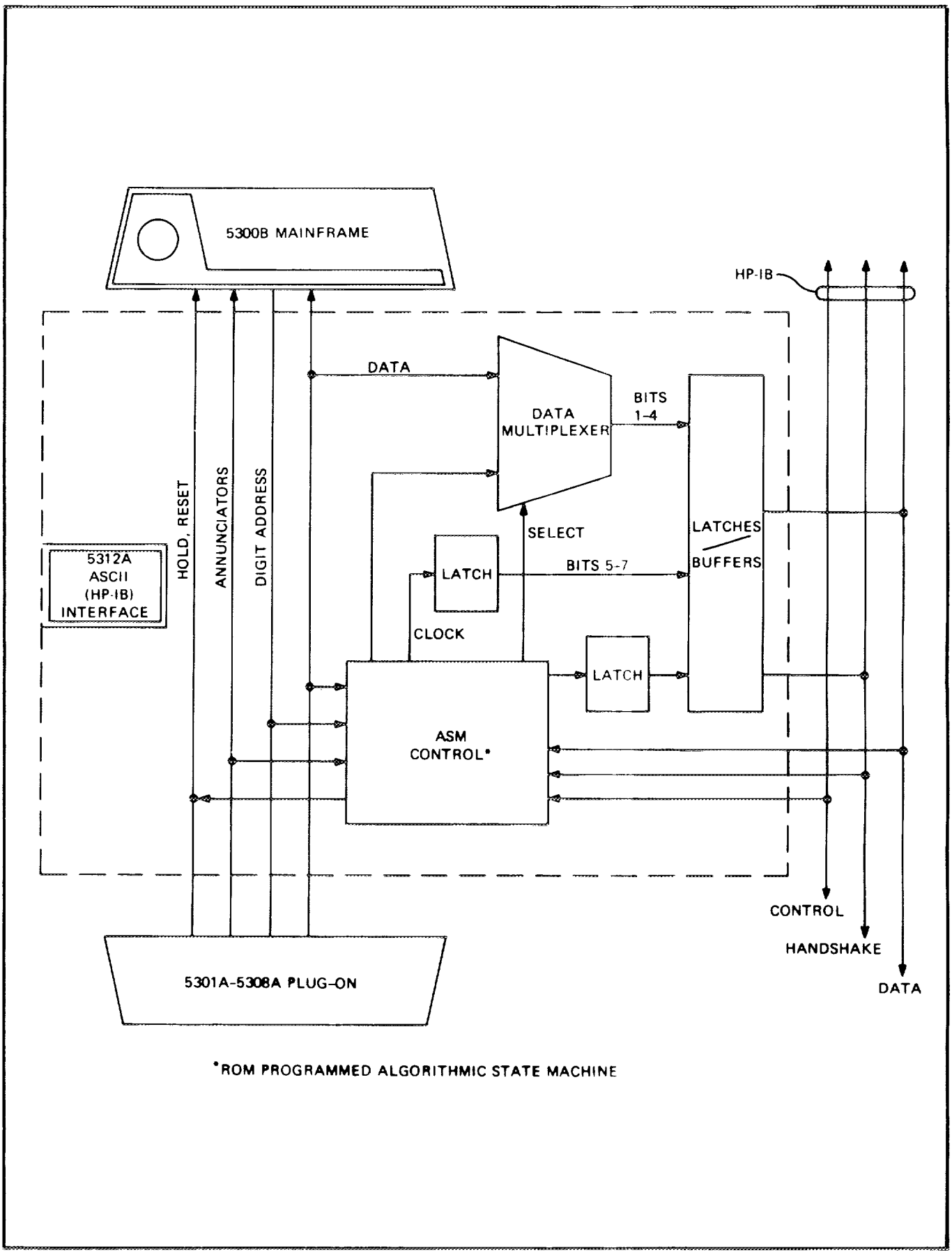


Figure 9L-4-1. Overall Block Diagram

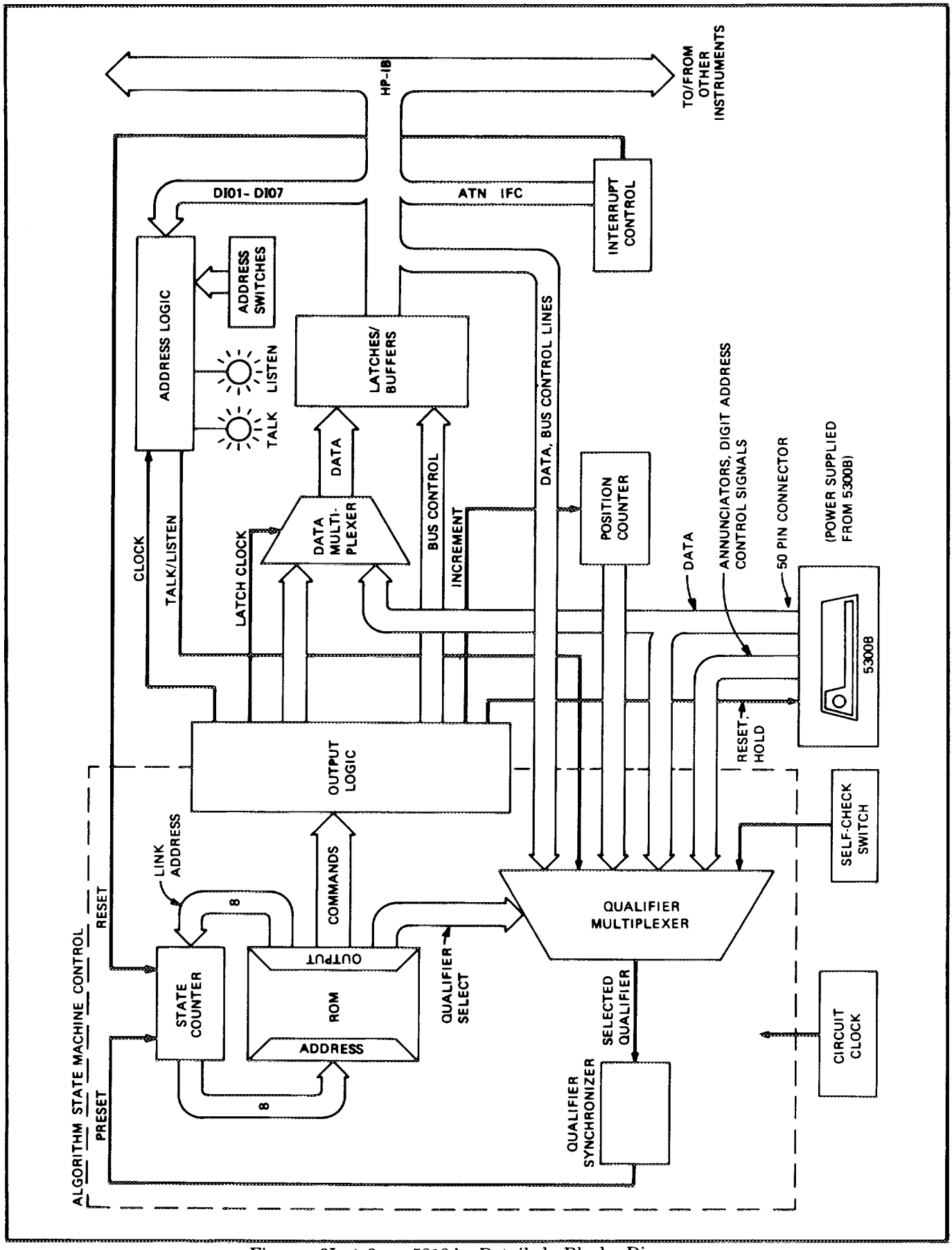


Figure 9L-4-2. 5312A Detailed Block Diagram

9L-4-13. The Position (P) Counters provide four outputs (P1, P2, P3, and P4) as qualifiers to the Qualifer Multiplexer. The logic state of the P qualifiers determines which character of the talk output format is sent to the HP-IB. The Position Counters are incremented by a signal from the Output Logic circuit.

9L-4-14. The Interrupt Control circuit processes the HP-IB Interface Clear (IFC) and Attention (ATN) signals to control the 5312A. The IFC signal resets the Talk and Listen FFs in the Address Logic circuit and resets the State Counters and the Position Counters. The ATN signal also resets the State Counters and Position Counters and in addition sets DAC low as required for proper operation on the HP-IB.

9L-4-15. The Circuit Clock is an RC oscillator that provides a CLK signal to clock the ASM operation and provides a $\overline{CLK}$ signal to enable the Output Logic circuits.

9L-4-16. DETAILED CIRCUIT DESCRIPTION

9L-4-17. The following paragraphs describe the circuits in detail as shown in the schematic diagram in Figure 9L-8-1.

9L-4-18. Address Logic

9L-4-19. The Address Logic circuit consists of an Address Comparator (U5), a Talk FF (U4), a Listen FF (U3), and a Trigger circuit (U9A,B).

9L-4-20. ADDRESS COMPARATOR, TALK FF AND LISTEN FF. The Address Comparator monitors the bus Data Input/Output (DIO) lines 1 through 5 and compares their logic states with the logic states of rear panel address switches 1 through 5, respectively. When a comparison occurs, the Address Comparator outputs the Address signal to the Talk FF and the Listen FF. The logic states of DIO lines 6 and 7 determine whether the Talk or Listen FF is set or reset when the Talk/Listen Clock (TLC) is received from ROM State Machine U11. The 5312A is in the Talk mode when the Talk FF is set and in the Listen mode when the Listen FF is set. The 5312A can be forced into the Talk mode, regardless of the state of the Talk FF, by setting the TALK ONLY switch open. This action allows the Talk FF output line to rise to +5V and simulate a set Talk FF condition.

9L-4-21. UNADDRESSING. The Unaddressed signal clears the Listen FF through gates U8A, B, and C, and U26A when DIO lines 1 through 5 are all logic 1's (approximately 0 volts). The Talk FF is cleared by any talk address except the address set on the rear panel address switch.

9L-4-22. TRIGGERING. The Trigger circuit monitors the DIO lines and responds to an Initiate command (ASCII "I" through U9A or to a Group Execute Trigger (ASCII backspace "BS") through U9B. Either trigger is processed by the State Machine to reset the mainframe to take a measurement.

9L-4-23. Algorithmic State Machine

9L-4-24. The Algorithmic State Machine (ASM) operation is similar to a microprocessor. It is programmed to control the output of measurement data from the 5300B mainframe to the HP Interface Bus. The ASM consists of 4K Read-Only-Memory (ROM) U11, State Counters U14 and U15, Qualifier Multiplexers U13, U10, U18, and U23, and associated circuits.

9L-4-25. ROM OPERATION. The 4K ROM outputs 16 bits. Seven of the output bits are used to address the Qualifier Multiplexers and are also sent to the Output Logic. Eight of the output bits are sent to the load inputs of the State Counters and are also sent to Data Multiplexers U12 and U16. The remaining bit is a Format (F) bit that determines the mode of operation of the State Machine (Decision Mode or Output Mode). Refer to Figure 9L-4-3. When the F bit is low (0) is allows the selected qualifier to enable the Preset Enable lines of the State Counters. This causes either an increment to the next line in the program or a jump to the link address at the next clock pulse. The decision to jump or not depends upon the state of the selected qualifier. When the F bit is high (1) the Preset Enable lines are turned off, all qualifiers are ignored, and the State Counters increment by one at each clock pulse. This mode of operation is the normal output mode of the ROM and the program proceeds in sequential order from one line number to the next.

9L-4-26. QUALIFIER MULTIPLEXERS. The four Qualifier Multiplexers each receive eight input qualifiers. The qualifiers are from the 5300 mainframe, the interface bus, or from internal circuitry. The logic state of the P1, P2, P3, and P4 outputs of the Position Counters are qualifiers that determine which character to output to the bus. Qualifiers are listed as follows:

DP1, DP2, DP3, DP4, DP5	Decimal Point lines from the mainframe.
P1, P2, P3, P4	4 bits of the 5312A position counter. The logic state of these bits determines which character to output to the bus.
RFD, DAC, DAV	The state of the HP-IB handshake lines. Ready for Data (RFD, Data Accepted (DAC) and Data Valid (DAV).
HATN	The inverted state of the attention (ATN) line.
X, Y, Z	The digit address lines of the mainframe.

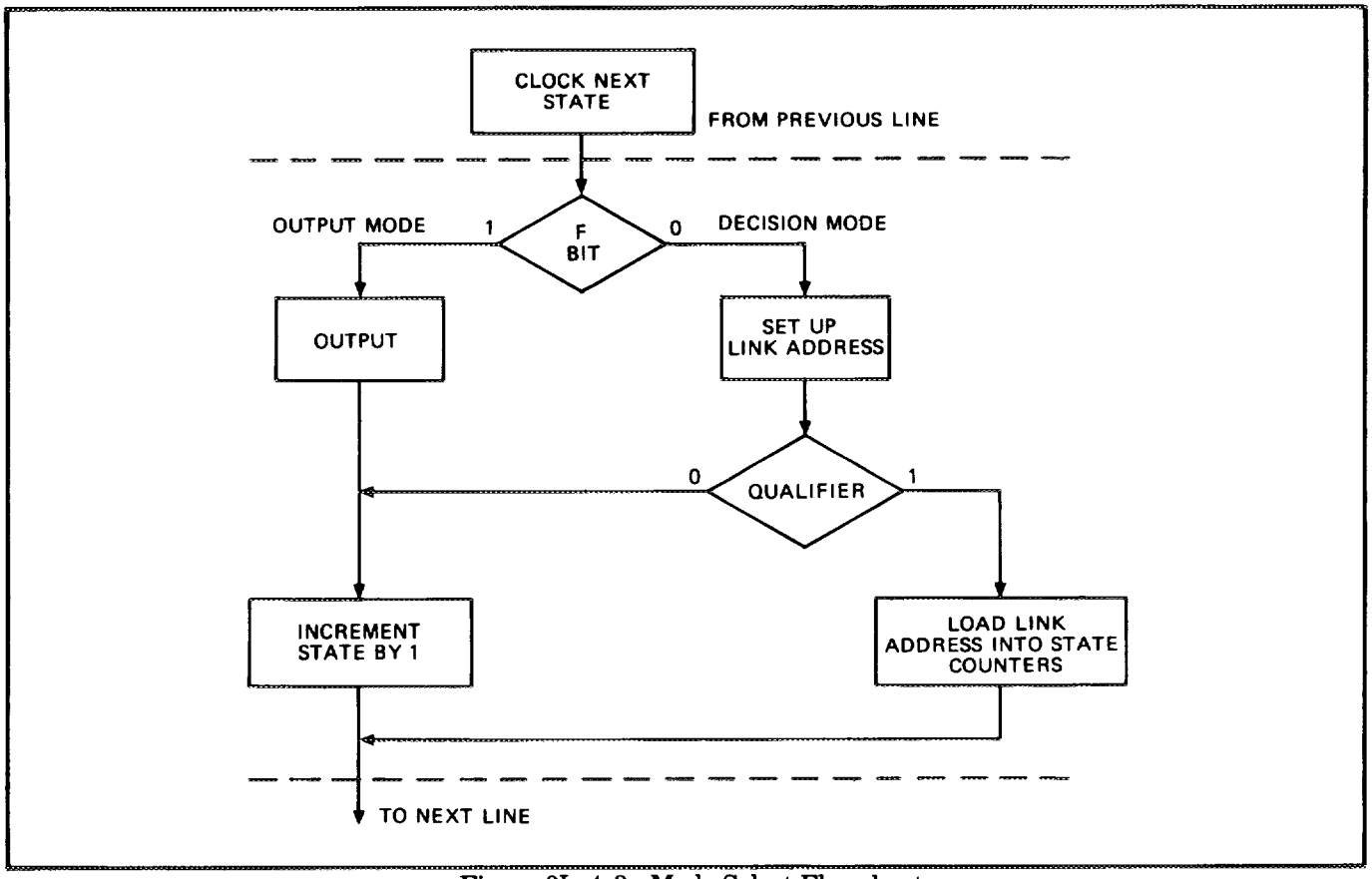


Figure 9L-4-3. Mode Select Flowchart

B	The data B line of the mainframe.
CD	The NAND of the C and D lines of the mainframe.
INHB	The inhibit line of the mainframe.
R/L	The Right/Left strobe line of the mainframe.
HLD	The Hold line of the mainframe.
S, K, μ, M, Hz	The annunciators of the mainframe.
OF	The overflow line of the mainframe.
INIT•TRIG	NAND of bits 7, 6, and 1 of the bus data lines.
INIT	NAND of bits 2, 3, 5, and NOT 4 of the bus lines. The INIT•TRIG and INIT qualifiers sense the Group Execute Trigger command to develop INIT•TRIG and sense the Initiate command to develop INIT.
LSN, TLK	Listen and Talk FF outputs.
SELF TEST	Test switch, used to implement self testing.

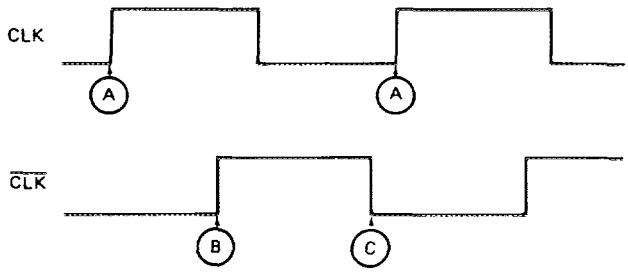
9L-4-27. The qualifier selected by the ROM program is sent to the Qualifier Control circuit.

9L-4-28. Qualifier Control

9L-4-29. The Qualifier Control circuit consists of gates U25A, U24B, Flip-Flop U28A and gate U19D. The output of the Qualifier Multiplexer sets the Qualifier FF (U28A). When the F bit from the ROM is high, an enable signal is sent to the Preset Enable of the State Counters (U14 and U15). This causes a conditional jump in the program as described in paragraph 9L-4-25. Flip-flop U28B receives a State Reset signal from the Interrupt Control circuit to reset the State Counters to zero.

9L-4-30. Circuit Clock

9L-4-31. The Circuit Clock is comprised of U19A, B, and C, and associated components connected as an RC oscillator. The CLK output is provided to the State Counters. The $\overline{CLK}$ output is supplied to Main Output Enable gates U24A, C, and to the Qualifier FF. The clock frequency is approximately 150 kHz and the phase relationship between the CLK and $\overline{CLK}$ outputs is as follows:



NOTE

At point A the State Counters are either advanced by 1 count or preset to the link address. This is the start of each state address. From points A to B the output from the ROM is allowed to settle to assure a steady signal. At point B, the main Output Enable gates are allowed to go active if the F bit and enable signals from the ROM are high. In addition, at point B the Qualifier FF will be set by a selected qualifier.

9L-4-32. Output Logic

9L-4-33. The Output Logic circuit receives and processes the instructions from the Algorithmic State machine. The outputs are provided to the interface bus and control signals are sent to the 5300B mainframe. The signals are grouped as Group 1, Group 2A, and Group 2B as follows:

GROUP 1

R_A, R_B, R_C, R_D — Serve as the four-least-significant bits of each ASCII output character from the ROM. Sent through LSB Latch U16 and transistors Q7-Q10 to the DIO lines.

R5, R6, R7 — Serve as the three-most-significant bits of each ASCII output character from the ROM. Sent through MSB Latch U12 and transistors Q4-Q6 to the DIO lines.

D/R — Data or ROM. This signal, when high, switches the quad two-input multiplexer inside U16 to accept data from the 5300B. When this signal is low, U16 accepts data from the ROM. This data will not be seen at the outputs until the LC line is pulsed. (LC is described in Group 2B below).

GROUP 2A

TLC — Talk/Listen FF clock from U8D. When the program realizes that an address is on the bus, it will pulse this line.

RMR — ROM controlled manual reset from U20B. This line, when pulsed, will reset the 5300B.

HLD1 — Hold "on" from U20A. This turns on the Hold line of the 5300B and is kept on by the Hold FF U17A, U25D.

HLD0 — Hold "off" from U25C. This clears the Hold FF.

GROUP 2B

LC — Latch Clock from U21D. This line, when pulsed, will clock U12 and U16 and will latch any data at the inputs of these IC's to the outputs. (Refer to D/R in Group 1 above.)

RDAV — ROM Data Valid from U21A. This line will set DAV FF U17C, D. A signal from LC will clear the FF.

RRFD — ROM Ready for Data from U21B. Sets RFD FF U17B, U22A and also clears the DAC FF.

RDAC — ROM Data Accepted from U21C. Set DAC FF U22B, C, and also clears the RFD FF.

INC — Increment from U25B. Increments the Position Counters U1 and U6 one count.

9L-4-34. ROM OUTPUT. The ROM outputs 16 bits of information for each state. One of these bits, labelled the Format bit or F bit, is used to determine how the other 15 bits are handled. If the F bit equals a 1, the word is handled as an Output word as described in paragraph 9L-4-25. With the requirement that the clock and enable signals from the ROM are met, the gates U24A or U24C can be turned on. A low signal from U24A enables outputs TLC, RMR, HLD1 and HLDØ. A log signal from U24C enables outputs LC, RDAV, RDAC, and INC. As an example, to pulse the INC output, the $\overline{CLK}$, F bit and 0_4 from the ROM must be high and 0_8 from the ROM must be low.

9L-4-35. Group 1 signals are fully parallel and come from the ROM in positive logic. Any combination of Group 1 signals is possible and is completely independent of Group 2 signals. Group 2 signals are partially parallel and within each set (A or B) are fully parallel. Only one set may be active at a time.

9L-4-36. OUTPUT TO BUS. The lower four bits of the ASCII character output to the bus can be selected from the ROM or from the 5300B mainframe by LSB Latch U16. This arrangement allows characters such as "E" or "+" to come from the ROM and allows measurement data to come from the mainframe. The three higher order bits are always supplied by the ROM because, in ASCII code, these higher order bits determine the interpretation of the lower four bits. For example, when numerical data is coming from the mainframe, bits 5, 6, and 7 will indicate that the data is numerical.

9L-4-37. The DAV FF (U17C,D), RF FF (U22A, U17B), and DAC FF (U22C,B) control the transfer of data on the bus. The RFD and DAC FF's are interconnected so that when one is set the other is cleared. However, both FFs may be cleared at the same time, for example, when the 5312A is a talker or when ATN is high. If the 5312A is a listen or when ATN is low, gate U20C is inactive and the RFD and DAC FFs will be controlled by the ROM. The DAV FF is cleared by the LC signal because the MSB and LSB Latches are cleared after each data transfer and data is no longer valid.

9L-4-38. Position Counters

9L-4-39. The Position Counters determine which talk output character is sent to the bus. The P1, P2, P3, and P4 qualifiers are sent to Qualifier Multiplexer U23 from Position Counters U1A, U1B, U6A, and U6B, respectively. The Position Counters are incremented by the INC signal from gate U25B. The logic state of the Position Counter outputs for each type of character in the talk output format is described in paragraph 9L-4-56.

9L-4-40. Interrupt Control

9L-4-41. The Interrupt Control circuit processes bus control signals Interface Clear (IFC) and Attention (ATN).

9L-4-42. IFC SIGNAL. The IFC signal clears all talkers and listeners on the bus. In the 5312A, IFC resets the State Counters to zero, resets the Talk FF, the Listen FF and the Position Counters. The IFC signal is received at gate U26C, buffered and fed to an RC filter that filters noise spikes on the line. The signal is inverted and buffered and sent to the Clear input of the Listen and Talk FFs. The signal is also applied to gate U26D and used to reset the State Counters U14 and U15. In addition, the Position Counters are reset via U27E and U2D. The IFC signal is simulated at power turn-on by the RC circuit connected to the input of U26C.

9L-4-43. ATN SIGNAL. When the ATN signal goes low it must also reset the State Counters and Position Counters. In addition, the DAC signal must go low immediately to prevent indicating to a controller that the 5312A has accepted data at this point. The ATN signal is sent through gate U27C to an RC filter, then through gate U27B to a pulse-forming network. The pulse is sent through U26D to reset the State Counters and Position Counters. However, since the signal is a pulse, the State Counters will be free to operate after several microseconds. In the case of the IFC signal, the State Counters are held at state zero until the signal changes state. The output of U27C disables U20C and the pulsed ATN signal goes to U22B through U26B. This combination of signals assures that DAC will go low as required when ATN goes low.

9L-4-44. PROGRAM OPERATION

9L-4-45. The operation of the 5312A is controlled by the Algorithmic State Machine program. The program consists of 256 lines (0-255) and is divided into three sections. The first section is the Data Transfer (Handshake) section shown in operational flowchart Figure 9L-8-2 (Sheet 1 of 3). The second section is the Output Data section shown in the flowchart (Sheet 2 of 3) and the third section is the Self Check section shown in the flowchart (Sheet 3 of 3).

9L-4-46. Conditional jumps in the program are described in paragraph 9L-4-25. These jumps are made as a test of a program condition. Unconditional jumps in the program are made by using a qualifier for a known condition. For example, when the 5312A is in the talk mode the TALK (TLK) qualifier is used, in the listen mode the LISTEN (LSN) qualifier is used. Each jump condition is shown as a decision diamond in the flowcharts. If the jump is shown as a loop or test condition, the jump is conditional. All other jumps are unconditional as shown by the qualifier. The decision blocks on all flowcharts lead into the next sequential line number of the program if the qualifier logic state is "0", or a jump if the logic state is "1", as shown in the flowchart. The number adjacent to each decision diamond or instruction square in the flowcharts is the program line number. The number on the right side is the decimal number and the number in parenthesis is the octal conversion such as 8 (010).

9L-4-47. Program operation is described in the following paragraphs in reference to the operational flowcharts.

9L-4-48. Data Transfer (Handshake)

9L-4-49. The Data Transfer (Handshake) operational flowchart is shown in Figure 9L-8-2 (Sheet 1 of 3). This description refers to the decimal number of the line in the program (the octal number conversion is also shown on the flowchart, in parenthesis).

9L-4-50. ADDRESSING. When ATN goes low, the State Counters are temporarily reset to Ø. When the pulsed ATN signal releases the counters, line Ø of the program will have cleared all the outputs (LC) and set up the RFD signal. (Refer to paragraph 9L-4-33 for signal descriptions.) Line 1 tests ATN which will still be low, and line 6 waits for DAV to go low. When the DAV line goes low, the program checks to see if the command on the bus is a Group Execute Trigger (lines 8, 9) and if so, are we a listener (line 10)? If true, we reset the 5300B and latch the Hold line "on" (line 16). Lines 17, 18, and 19 make sure that a new measurement was started.

9L-4-51. If the data was an address, the Talk and Listen flip-flops are clocked (line 11) and signal that the data was accepted (line 12). We then wait for the DAV signal to go back high and return for a new cycle

or address (lines 13, 14, 15). If the command was neither the GET command or an address, the flip-flops will not be affected by the TLC pulse (line 11). If it was a correct address, the 5312A will now be either a listener or a talker.

9L-4-52. INITIATE COMMAND. The 5300B can be reset with the GET from a controller or by an Initiate (I) command from a Talker. In this case, the 5312A must first be addressed as a Listener, as before, and then some other instrument on the bus must be addressed as a Talker (not necessarily in this order). Then when ATN goes high, the program will end up at line 20 waiting for the Talker to pull DAV low (RFD will have been set by line Ø). When DAV goes low, the program checks to see if the command on the lines is an Initiate Command for the 5300B (line 21); if not, we jump to line 12 to complete the handshake. If it was an Initiate Command, go to line 16 to reset the mainframe.

9L-4-53. When the 5312A is addressed as a Talker and ATN goes high, the program will end up in line 21 waiting for listeners to say they are ready for data. If RFD is high and DAV is also high, this means that no one is connected as a listener and we default and wait for a valid situation (lines 25, 181, 182). The Hold line will be cleared to allow the instrument to free run in this case.

9L-4-54. Assuming that there is a listener on the bus, DAC should be low. Then line 26 checks to see if a measurement was previously triggered, or if we must wait for a new one. If the Hold line is low, it means a measurement was triggered and we go to line 27 to wait for Inhibit to go low, thus signaling that the measurement is completed. If the Hold line is high, we must wait for the Inhibit line to go high, then low (lines 45, 46, 26) to assure a good measurement has taken place. In line 28, Hold goes low to latch the measurement. If the Hold line is already low, it will make no difference.

9L-4-55. Output Mode

9L-4-56. To output each character of the output word onto the data lines, the program checks the 4-bit Position Counter outputs. Table 9L-4-1 shows Position Counter output logic states for each output character. The paragraphs that follow described the program flow for each output character.

9L-4-57. OUTPUT 1ST CHARACTER ($^{P4}_{1}\ ^{P3}_{1}\ ^{P2}_{0}\ ^{P1}_{1}$). From line 28 of the program shown in Sheet 1 of Figuure 9L-8-2, go to line 29 at the top of Sheet 2. Since P4 IS A "1", go to line 114 and check P3 for a "1". This leads to P1 which is a "1" in line 119. Since P1 is a "1", go to line 128 and check P2 for a "0". Go to line 129 and check the overflow line. If overflow is low, output the letter "O" onto the bus and latch it (line 130). Return to line 47 (Sheet 1) to complete the handshake (data transfer) for this byte. If overflow is high, go to line 112 and output a space, then return to line 47. The same procedure is followed for each succeeding character as described in the following paragraphs.

Table 9L-4-1. Position Counter Outputs

Output Order	P4	P3	P2	P1	Output Character
1	1	1	0	1	Space or O for overflow
2	1	1	1	0	H, S, V, R, or Space for function code
3	1	1	1	1	Space
4	0	0	0	0	Space if there is no decimal point. Also MSD of data.
5	0	0	0	1	Space/next digit
6	0	0	1	0	Minus sign or digit
7	0	0	1	1	Digit and/or decimal point
8	0	1	0	0	Digit and/or decimal point
9	0	1	0	1	Digit and/or decimal point
10	0	1	1	0	Digit and/or decimal point
11	0	1	1	1	Digit and/or decimal point
12	*	*	*	*	(P Counters not incremented for decimal point)
13	1	0	0	0	E
14	1	0	0	1	+ or -
15	1	0	1	0	0, 3, 6, or 9
16	1	0	1	1	Carriage Return
17	1	1	0	0	Line Feed

9L-4-58. OUTPUT 2ND CHARACTER ($^{P4}_{1}\ ^{P3}_{1}\ ^{P2}_{1}\ ^{P1}_{0}$). This leads to line 132 to check the Hz line. If this line is low, output an F (lines 133, 134). If not, check the Seconds line (135). If this line is low, output an S (lines 136, 137). If it is neither of these two, we must assume that it is a totalize, ratio, voltage, or ohms measurement. To find out which, we must look at the 6th most-significant-digit where the minus sign would appear. First, lines 138, 139, 140, and 141 synchronize with the R/L line to assure that we are looking at the digit address lines during the middle of a cycle (double testing is used to assure reliability). Then, once synchronized, we check to see if it is the 5th digt. If it is not, we go back to line 138 to resynchronize (lines 142, 143, 144, 145, 146). If it is the 5th digit, line 147 will check to see if it is a digit or not. If it is a digit, the measurement is a totalize or ratio and we output a space (line 112). If the 5th digit is a space or minus sign, we check the annunciators to see if the measurement is volts or ohms. We can distinguish volts from ohms by knowing that ohms always illuminates a K or an M and volts do not. Therefore, lines 148, 151, and 152 check for this. We eventually output a V or R (lines 153, 154, 149, 150).

9L-4-59. OUTPUT 3RD CHARACTER ($^{P4\ P3\ P2\ P1}_{1\ 1\ 1\ 1}$). The third character is always a space (lines 128, 112).

9L-4-60. OUTPUT 4TH CHARACTER ($^{P4\ P3\ P2\ P1}_{0\ 0\ 0\ 0}$). To keep the number of characters in the output consistent, we must compensate with a space whenever there is no decimal point in the display. Lines 31 through 41 check to see if there is a decimal point present. If none exist, a space is put on the lines and we go to line 95 to the decimal point data transfer (handshake). This decimal point handshake is basically the same as the handshake used for all the other characters, but unlike the "main" handshake, this one will not increment the P counters when finished). (The handshake consisting of lines 23 to 52 is the "main" handshake. It is the common handshake used for all the other characters.)

9L-4-61. Note that line 47 turns on both DAV and DAC. DAV is to signal that the data is valid, usual for a talker. The DAC signal is there to assure that the DAC line is high (the equivalent of off) just in case the 5312A was also addressed to listen and the gating (U20C in Figure 9L-8-1) did not disable this line. This is referred to as "listening to itself". Lines 95 to 100 form the standard handshake. Lines 183, 184, and 185 feed control to the normal digit routine (69) if we arrived at this point from outputting a decimal point. If we got here from outputting a space (41), we are transferred to line 53.

9L-4-62. OUTPUT 5TH CHARACTER ($^{P4\ P3\ P2\ P1}_{0\ 0\ 0\ 1}$). This character position routes the program first through a detection routine, and then to either an output-space routine or output-digit routine. It is similar to the 0000 scheme except that compensation for "no decimal point" is not checked or needed here.

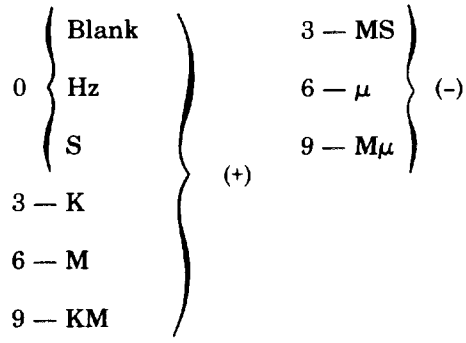
9L-4-63. OUTPUT 6TH CHARACTER ($^{P4\ P3\ P2\ P1}_{0\ 0\ 1\ 0}$). This position will either print a digit, space, or minus sign. It goes directly to the comparator routine (line 69) and drops down to output one of the possibilities depending upon which plug-on is installed.

9L-4-64. OUTPUT 7TH, 8TH, 9TH, 10TH, AND 11TH CHARACTERS (P4, P3, P2, and P1 EQUALS 0011, 0100, 0101, 0110, and 0111, RESPECTIVELY. In each of these positions, the program checks to see if a decimal point is needed and then (whether one is outputted or not) proceeds with also putting a digit on the lines.

9L-4-65. The decimal point detection is accomplished at lines 93, 103, 104, 108, 109, 106, 107, 110, and 111. The decimal point selected depends upon the digit position. If a decimal point exists, the program will output the decimal point and handshake the data. It will not increment the Position Counters because the digit has not been selected yet. When the handshake is completed for the decimal point, go to line 69 to look for a digit. If no decimal point exists for any particular position, we go directly to the digit comparator routine (line 69). The fact that the Position Counters are not incremented for decimal points explains the asterisks (****) in Table 9L-4-1 for the 12th character.

9L-4-66. OUTPUT 13TH CHARACTER ($^{P4\ P3\ P2\ P1}_{1\ 0\ 0\ 0}$). The 13th character always outputs an E (line 117).

9L-4-67. OUTPUT 14TH CHARACTER ($^{P4\ P3\ P2\ P1}_{1\ 0\ 0\ 1}$). The 14th character is a plus or minus according to this list (the decision tree starting at line 155 determines the sign):



9L-4-68. OUTPUT 15TH CHARACTER ($^{P4\ P3\ P2\ P1}_{1\ 0\ 1\ 0}$). The 15th character is a 0, 3, 6, or 9 according to the list in the preceding paragraph. The decision tree for this starts at line 164.

9L-4-69. OUTPUT 16TH CHARACTER ($^{P4\ P3\ P2\ P1}_{1\ 0\ 1\ 1}$). The 16th character always outputs a carriage return.

9L-4-70. OUTPUT 17TH CHARACTER ($^{P4\ P3\ P2\ P1}_{1\ 1\ 0\ 0}$). The 17th character always outputs a linefeed. However, the second half of the handshake is done here (lines 122, 123, 124) so that after it is completed, the program can release the Hold line (125). Lines 126 and 127 double check to make sure hold is reset. Lines 47 to 50 complete the handshake that started in lines 21, 22, 23. Line 51 increments the Position Counters to the next position and also clears the output latches. Line 4 checks to see if we are in the self check mode, described in the following paragraph.

9L-4-71. Self Check

9L-4-72. The Self Check operational flowchart is shown in Figure 9L-8-2, Sheet 3 of 3. The Self Check starts at program line number 186 (decimal), 272 (octal) as shown in the flowchart. Procedures for performing the Self Check are described in paragraph 9L-3-32. Use of the Self Check for troubleshooting is described in paragraph 9L-5-19.

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION V
MAINTENANCE

9L-5-1. INTRODUCTION

9L-5-2. This subsection contains maintenance information for Model 5300B/5312A ASCII Interface. Performance checks, maintenance procedures, and tests to isolate defective components are included.

9L-5-3. RECOMMENDED TEST EQUIPMENT

9L-5-4. Test equipment recommended for performance checking and servicing the 5300B/5312A is listed in Table 9L-5-1 and in Table 5-1 in the 5300B portion of the manual. Test equipment with equivalent characteristics may be substituted for listed equipment.

9L-5-5. INSTRUMENT ACCESS

9L-5-6. For access to the 5312A plug-between assembly refer to the installation and removal procedures, paragraph 9L-2-7.

9L-5-7. MAINTENANCE AND REPAIR

9L-5-8. General procedures for board removal, component replacement and integrated circuit replacement are described in Section V of the 5300B portion of the manual.

Table 9L-5-1. Recommended Test Equipment

Instrument Type	Required Characteristics	Recommended Instruments
Calculator	HP-IB Controller	HP 9820A/ 9821A/ 9830A
Logic Clip	Indicate logic levels	HP 10528A
Logic Probe	Indicate logic levels	HP 10525T

9L-5-9. VERIFICATION OF PERFORMANCE

9L-5-10. To quickly verify the performance of the 5312A, perform the self check procedure in paragraph 9L-3-33. A more extensive method to verify the performance on the HP-IB is to use the 9820A/21A or 9830A Calculator as described in the following paragraphs.

9L-5-11. Verification Using 9820A/21A Calculator

NOTE

It is assumed that a system including the 9820A/21A Calculator, the ASCII Interface and Peripheral Control II, and the 5300B/5312A/5301A-5308A plug-on (with the 5312A address switches set to 01010 ADDRESSABLE and NORM) has been interconnected and prepared for operation. (Operate the plug-on in any mode except totalize mode of 5301A, 5302A, and 5304A.) For detailed operating procedures, refer to Peripheral Control II operating manual, HP Part No. 09820-90024 and HP-IB Users Guide 9820A/21A.

9L-5-12. LOADING THE PROGRAM. Prior to loading the program, push the END and EXECUTE keys. This positions the program counter to zero. Push the remaining keys to program the calculator as shown in the following printer list:

NOTE

This program checks the 5312A three times. First, the addressable non-triggered mode; second, the triggered initiate (I) command; third, the triggered Group Execute Trigger universal command. The calculator printout will depend upon the function of the plug-on. Printout codes are: 32 = SP (space), 70 = F (Frequency), 79 = O (Overflow), 82 = R (Resistance), 83 = S (Seconds), and 86 = V (Volts).

9820A Calculator Program Printer List

```
0:
"S";CMD "?J5";
CSB "P";PRT "1ST
"⊢
1:
CMD "?U*","I","?
J5";GSB "P";PRT
"2ND"⊢
2:
CMD "?U*2(2?J5";
CSB "P";PRT "3RD
"⊢
3:
GTO "S"⊢
4:
"P";FMT *;RDB 13
→A;RDB 13→B;RED
13,C;FXD 0;PRT A
,B,C;RET ⊢
FXD 0
```

Typical Calculator Printout

```
1ST
                32
                70
          10000000
2ND
                32
                70
          10000000
3RD
                32
                70
          10000000
```

NOTE

The unusual symbol in line 2 of the above printer list is produced by the 9820A display key.

9L-5-13. VERIFYING THE PROGRAM. After the program has been loaded, push the END and LIST keys. This will run a printer list of the program. Check the list to verify that the program was entered correctly.

9L-5-14. RUNNING THE PROGRAM. To run the program push the END and RUN PROGRAM keys. Performance of the 5312A is verified when the calculator printout indicates the same value as the 5300B display. To end the program, push the STOP key.

9L-5-15. Verification Using 9830A Calculator

NOTE

It is assumed that a system including the 9830A Calculator, the ASCII Interface Card, the Extended I/O ROM, and the 5300B/5312A/5301A-5308A plug-on (with the 5312A address switches set to 01010 ADDRESSABLE and NORM) has been interconnected and prepared for operation. (Operate the plug-on in any mode except totalize mode of 5301A, 5302A, and 5304A.) For detailed operating procedures, refer to 9830A Operating and Programming Manual, HP Part No. 09830-90001, to the Extended I/O ROM Operating Manual, Part No. 09830-90007, and to HP-IB Users Guide 9830A.

9L-5-16. LOADING THE PROGRAM. Prior to loading the program, push the STOP key down until STOP appears on display. If display remains blank refer to the 9830A Operating and Programming Manual, Appendix A. Push the remaining keys to program the calculator as shown in the following program.

NOTE

This program checks the 5312A three times. First the addressable non-triggered mode; second, the triggered Initiate (I) command; third, the triggered Group Execute Trigger universal command. The calculator display will depend upon the function of the plug-on. Display codes are: 32 = SP (space), 70 = F (Frequency), 70 = O (Overflow), 82 = R (Resistance), 83 = S (Seconds), and 86 = V (Volts).

9830A Calculator Program

```
10 CMD "?J5"
20 N=1
30 GOSUB 140
40 CMD "?U*","I","?J5"
50 N=2
60 GOSUB 140
70 CMD "?U*"
80 FORMAT 3B
90 OUTPUT (13,80)256,8,512;
100 CMD "?J5"
110 N=3
120 GOSUB 140
130 GOTO 10
140 ENTER (13,150)O,F,D
150 FORMAT 2B,E16.8
160 DISP "#";N;O;F;D
170 WAIT 4000
180 RETURN
```

Typical Display Data

#1 32 70 10 000 000
#2 32 70 10 000 000
#3 32 70 10 000 000

NOTE

Data is displayed in basic units such as Hz, seconds, etc.

9L-5-17. VERIFYING THE PROGRAM. After the program has been loaded, push the FETCH and EXECUTE keys. This will display the first line of the program. Then use DISPLAY keys to verify that the program was entered correctly.

9L-5-18. RUNNING THE PROGRAM. To run the program push the RUN and EXECUTE keys. Performance of the 5312A is verified when the calculator displays the same value as the 5300B. To end the program, push the STOP key.

9L-5-19. TROUBLESHOOTING

9L-5-20. Use the following troubleshooting information, the Self Check Flowchart, Figure 9L-8-2 and the schematic diagram, Figure 9L-8-1 to isolate troubles in the 5312A to a defective component.

9L-5-21. GENERAL. When operating the 5312A (connected to a known good 5300B and plug-on module) and a trouble is indicated, analyze the front panel display and indicators for evidence of trouble symptoms. When a symptom is determined, refer to the Self Check Flowchart, Figure 9L-8-2, Sheet 3. The binary numbers that are enclosed in a box at various points in the flowchart indicate the status of the Position Counters. The P1, P2, P3, and P4 output is indicated by a logic 1 or logic 0. The program line number shown in the flowchart adjacent to each diamond or square indicates the address of the State Machine at that point in the program. This number indicates the logic state of the State Counter outputs and is shown in decimal form on the right side with the octal conversion on the left in parenthesis. The outputs of the Position Counters and the State Counters are connected to a dummy IC (no internal circuitry) which is labeled STATE ADDRESS TEST IC. The connections are shown in the schematic diagram in Figure 9L-8-1. This test IC (U7) provides a connection for a logic clip or logic analyzer to indicate the logic states of the Position Counter and State Counter outputs during the Self Check. If the Program stops in a loop at any point in the program, the logic clip or analyzer will indicate (in binary form) the program line number where the stop occurred. The binary number can be converted to octal to locate the point where the malfunction occurred and allows isolation of the circuit trouble.

9L-5-22. PROCEDURES. Specific procedures for troubleshooting the 5312A are as follows:

NOTE

The following procedures are performed using Test Card "A", Test 4 as described in Section V of the 5300B portion of the manual. Test Card B, Test 7 may be used as a substitute method but the right-most digit of the 5300B display must be a stable zero which may be difficult to accomplish using Test 7. If test cards are not available, an alternate method may be used as described in Section V of the 5300B portion of the manual, paragraph 5-48. A 50-pin connector, used in place of the test card, is hard wired per Table 5-2, Test 4.

a. With power off, connect the 5312A to a 5300B without a plug-on module installed.

b. Insert Diagnostic Test Card "A" through Interface Card, HP Part No. 05300-60004 to 5312A 50-pin connector J1. Insert side of card marked "Test 4".

c. Remove shield plate and connect a 10528A Logic Clip to STATE ADDRESS TEST IC (U7) on the 5312A.

d. Disconnect the HP-IB cable if connected to the 5312A.

e. Set the switches on the rear panel of the 5312A to the following positions:

1. Press all address switches (A1-A5) to 0 (bottom pressed in).

2. Press the TALK ONLY/ADDRESSABLE switch to ADDRESSABLE position.

3. SHIELD switch in either position.

4. Press SELF CHECK switch to SELF CHECK position.

5. Reset the 5312A by turning the power off (on 5300B) then back on with a firm motion.

NOTE

The Self Check will not operate properly unless the right-most digit on the display is a zero.

f. Correct operation of the 5312A is indicated as follows:

1. The 5300B display is illuminated with an 8 in each digit position, decimals in the 5 right-most positions and overflow.

2. The TALK indicator is illuminated.

g. If indications are incorrect (5300B display cycles from all 0's through all 9's), observe the logic states shown on the Logic Clip to determine where the program stopped (shown in the flowchart, Figure 9L-8-2, Sheet 3).

NOTE

Pins 1 through 8 of test IC (U7) show the output of State Counters U14 and U15 in binary form, which is the program line number. Convert this number to octal to locate the point in the flowchart where the program stops or loops. (Octal numbers are shown in parenthesis in the flowchart). The logic state of the Position Counters (P1, P2, P3, and P4) is shown in the small squares adjacent to program blocks. The state of P1, P2, P3, and P4 is shown on U7 pins 12, 11, 10, and 9, respectively. The connections are shown in the schematic diagram, Figure 9L-8-1.

h. After isolating the problem area on the flowchart, refer to the schematic diagram, Figure 9L-8-1 to further isolate the problem to a component.

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION VI
REPLACEABLE PARTS

9L-6-1. INTRODUCTION

9L-6-2. This subsection contains information for ordering replacement parts. Table 9L-6-1 lists parts used in the 5312A in alphanumeric order of their reference designators and provides the following information for each part. Miscellaneous parts are listed at the end of Table 9L-6-1.

a. Hewlett-Packard part number.

b. Description of part (see abbreviations below).

c. Total quantity used in the instrument (shown only after the first entry for a given part).

d. Typical manufacturer of the part in a five-digit code (see list of manufacturer's in Table 9L-6-2).

e. Manufacturer's part number.

9L-6-3. ORDERING INFORMATION

9L-6-4. To obtain replacement parts, address order to your local Helwett-Packard Sales and Service Office (see lists at the back of the 5300 manual for addresses). Identify parts by their Hewlett-Packard part number. To obtain a part that is not listed, include:

a. Instrument model number.

b. Instrument serial number.

c. Description of the part.

d. Function and location of the part.

REFERENCE DESIGNATIONS

A	= assembly	E	= miscellaneous electrical part	MP	= miscellaneous mechanical part	TP	= test point
AT	= attenuator; isolator; termination	F	= fuse	P	= electrical connector (movable portion); plug	U	= integrated circuit; microcircuit
B	= fan; motor	FL	= filter	Q	= transistor; SCR; triode thyristor	V	= electron tube
BT	= battery	H	= hardware	R	= resistor	VR	= voltage regulator; breakdown diode
C	= capacitor	HY	= circulator	RT	= thermistor	W	= cable; transmission path; wire
CP	= coupler	J	= electrical connector (stationary portion); jack	S	= switch	X	= socket
CR	= diode; diode thyristor; varactor	K	= relay	T	= transformer	Y	= crystal unit-piezo-electric
DC	= directional coupler	L	= coil; inductor	TB	= terminal board	Z	= tuned cavity; tuned circuit
DL	= delay line	M	= meter	TC	= thermocouple		
DS	= annunciator; signaling device (audible or visual); lamp; LED						

ABBREVIATIONS

A	= ampere	BCD	= binary coded decimal	COMP	= composition	°K	= degree Kelvin
ac	= alternating current	BD	= board	COMPL	= complete	DEPC	= deposited carbon
ACCESS	= accessory	BE CU	= beryllium copper	CONN	= connector	DET	= detector
ADJ	= adjustment	BFO	= beat frequency oscillator	CP	= cadmium plate	diam	= diameter
A/D	= analog-to-digital	BH	= binder head	CRT	= cathode-ray tube	DIA	= diameter (used in parts list)
AF	= audio frequency	BKDN	= breakdown	CTL	= complementary transistor logic	DIFF AMPL	= differential amplifier
AFC	= automatic frequency control	BP	= bandpass	CW	= continuous wave	div	= division
AGC	= automatic gain control	BPF	= bandpass filter	cw	= clockwise	DPDT	= double-pole, double-throw
AL	= aluminum	BRS	= brass	D/A	= digital-to-analog	DR	= drive
ALC	= automatic level control	BWO	= backward-wave oscillator	dB	= decibel	DSB	= double sideband
AM	= amplitude modulation	CAL	= calibrate	dBm	= decibel referred to 1 mW	DTL	= diode transistor logic
AMPL	= amplifier	ccw	= counterclockwise	dc	= direct current	DVM	= digital voltmeter
APC	= automatic phase control	CER	= ceramic	deg	= degree (temperature interval or difference)	ECL	= emitter coupled logic
ASSY	= assembly	CHAN	= channel	...°	= degree (plane angle)	EMF	= electromotive force
AUX	= auxiliary	cm	= centimeter	°C	= degree Celsius (centrigrade)	EDP	= electronic data processing
avg	= average	CMO	= coaxial	°F	= degree Fahrenheit	ELECT	= electrolytic
AWG	= american wire gauge	COEF	= coefficient				
BAL	= balance	COM	= common				

ABBREVIATIONS (CONTINUED)

ENCAP	= encapsulated
EXT	= external
F	= farad
FET	= field-effect transistor
F/F	= flip-flop
FH	= flat head
FOL H	= fillister head
FM	= frequency modulation
FP	= front panel
FREQ	= frequency
FXD	= fixed
g	= gram
GE	= germanium
GHz	= gigahertz
GL	= glass
GND	= ground(ed)
H	= henry
h	= hour
HET	= heterodyne
HEX	= hexagonal
HD	= head
HDW	= hardware
HF	= high frequency
HG	= mercury
HI	= high
HP	= Hewlett-Packard
HPF	= high pass filter
HR	= hour (used in parts list)
HV	= high voltage
Hz	= Hertz
IC	= integrated circuit
ID	= inside diameter
IF	= intermediate frequency
IMPG	= impregnated
in	= inch
INCD	= incandescent
INCL	= include(s)
INP	= input
INS	= insulation
INT	= internal
kg	= kilogram
kHz	= kilohertz
kΩ	= kilohm
kV	= kilovolt
lb	= pound
LC	= inductance-capacitance
LED	= light-emitting diode
LF	= low frequency
LG	= long
LH	= left hand
LIM	= limit
LIN	= linear taper (used in parts list)
lin	= linear
LK WASH	= lockwasher
LO	= low, local oscillator
LOG	= logarithmic taper (used in parts list)
log	= logarithm(ic)
LPF	= low pass filter
LV	= low voltage
m	= meter (distance)
mA	= milliampere
MAX	= maximum
MΩ	= megohm
MEG	= meg (10^6) (used in parts list)
MET FLM	= metal film
MET OX	= metal oxide
MF	= medium frequency; microfared (used in parts list)
MFR	= manufacturer
mg	= milligram
MHz	= megahertz
mH	= millihenry
mho	= mho
MIN	= minimum
min	= minute (time)
'	= minute (plane angle)
MINAT	= miniature
mm	= millimeter
MOD	= modulator
MOM	= momentary
MOS	= metal-oxide semiconductor
ms	= millisecond
MTG	= mounting
MTR	= meter (indicating device)
mV	= millivolt
mVac	= millivolt, ac
mVdc	= millivolt, dc
mVpk	= millivolt, peak
mVp-p	= millivolt, peak-to-peak
mVrms	= millivolt, rms
mW	= milliwatt
MUX	= multiplex
MY	= mylar
μA	= microampere
μF	= microfarad
μH	= microhenry
μmho	= micromho
μs	= microsecond
μV	= microvolt
μVac	= microvolt, ac
μVdc	= microvolt, dc
μVpk	= microvolt, peak
μVp-p	= microvolt, peak-to-peak
μVrms	microvolt, rms
μW	= microwatt
nA	= nanoampere
NC	= no connection
N/C	= normally closed
NE	= neon
NEG	= negative
nF	= nanofarad
NI PL	= nickel plate
N/O	= normally open
NOM	= nominal
NORM	= normal
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NRFR	= not recommended for field replacement
NSR	= not separately replaceable
ns	= nanosecond
nW	= nanowatt
OBD	= order by description
OD	= outside diameter
OH	= oval head
OP AMPL	= operational amplifier
OPT	= option
OSC	= oscillator
OX	= oxide
oz	= ounce
Ω	= ohm
P	= peak (used in parts list)
PAM	= pulse-amplitude modulation
PC	= printed circuit
PCM	= pulse-code moudulation; pulse-count modulation
PDM	= pulse-duration modulation
pF	= picofarad
PH BRZ	= phosphor bronze
PHL	= Phillips
PIN	= positive-instrinsic-negative
PIV	= peak inverse voltage
pk	= peak
PL	= phase lock
PLO	= phase lock oscillator
PM	= phase modulation
PNP	= positive-negative-positive
P/O	= part of
POLY	= polystyrene
PORC	= porcelain
POS	= position; position(s) (used in parts list)
POSN	= position
POT	= potentiometer
p-p	= peak-to-peak
PP	= peak-to-peak (used in parts list)
PPM	= pulse-position modulation
PREAMPL	= preamplifier
PRF	= pulse repetition frequency
PRR	= pulse repetition rate
ps	= picosecond
PT	= point
PTM	= pulse-time modulation
PWM	= pulse-width modulation
PWV	= peak working voltage
RC	= resistance-capacitance
RECT	= rectifier
REF	= reference
REG	= regulated
REPL	= replaceable
RF	= radio frequency
RFI	= radio frequency interference
RH	= round head; right hand
RLC	= resistance-inductance-capacitance
RMO	= rack mount only
rms	= root-mean-square
RND	= round
ROM	= read-only memory
R&P	= rack and panel
RWV	= reverse working voltage
S	= scattering parameter
s	= second (time)
"	= second (plane angle)
S-B	= slow-blow (fuse (used in parts list)
SCR	= silicon controlled rectifier; screw
SE	= selenium
SECT	= sections
SEMICON	= semiconductor
SHF	= superhigh frequency
SI	= silicon
SIL	= silver
SL	= slide
SNR	= signal-to-noise ratio
SPDT	= single-pole, double-throw
SPG	= spring
SR	= split ring
SPST	= single-pole, single-throw
SSB	= single sideband
SST	= stainless steel
STL	= steel
SQ	= square
SWR	= standing wave ratio
SYNC	= synchronize
T	= timed (slow blow fuse)
TA	= tantalum
TC	= temperature compensating
TD	= time delay
TERM	= terminal
TFT	= thin-film transistor
TGL	= toggle
THD	= thread
THRU	= through
TI	= titanium
TOL	= tolerance
TRIM	= trimmer
TSTR	= transistor
TTL	= transistor-transistor logic
TV	= television
TVI	= television interference
TWT	= traveling wave tube
U	= micro (10^{-6}) (used in parts list)
UF	= microfarad (used in parts list)
UHF	= ultrahigh frequency
UNREG	= unregulated
V	= volt
VA	= voltampere
Vac	= volts ac
VAR	= variable
VCO	= voltage-controlled oscillator
Vdc	= volts dc
VDCW	= volts dc, working (used in parts list)
V(F)	= volts, filtered
VFO	= variable-frequency oscillator
VHF	= very-high frequency
Vpk	= volts peak
Vp-p	= Volts peak-to-peak
Vrms	= volts rms
VSWR	= voltage standing wave ratio
VTO	= voltage-tuned oscillator
VTVM	= vacuum-tube voltmeter
V(X)	= volts, switched
W	= watt
W/	= with
WIV	= working inverse voltage
WW	= wirewound
W/O	= without
YIG	= yttrium-iron-garnet
Zo	= characteristic impedance

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

Table 9L-6-1. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	05312-60001	1	INTERFACE ASSEMBLY	28480	05312-60001
A1C1	0160-2055	3	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
A1C2	0180-1702	1	CAPACITOR-FXD; 180UF+-20% 6VDC TA-SOLID	56289	150D187X0006R2
A1C3	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
A1C4	0160-3879	5	CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
A1C6	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1C7	0140-0193	1	CAPACITOR-FXD 82PF +-5% 300WVDC MICA	72136	DM15E820J0300WV1CR
A1C8	0160-0336	2	CAPACITOR-FXD 100PF +-1% 300WVDC MICA	28480	0160-0336
A1C9	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1C10	0180-1701	1	CAPACITOR-FXD; 6.8UF+-20% 6VDC TA-SOLID	56289	150D685X0006A2
A1C11	0160-0336		CAPACITOR-FXD 100PF +-1% 300WVDC MICA	28480	0160-0336
A1C12	0160-0945	1	CAPACITOR-FXD 910PF +-5% 100WVDC MICA	28480	0160-0945
A1C13	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1C14	0160-2197	1	CAPACITOR-FXD 10PF +-5% 300WVDC MICA	28480	0160-2197
A1C15	0160-3879		CAPACITOR-FXD .01UF +-20% 100WVDC CER	28480	0160-3879
A1CR1	1902-0031	1	DIODE-ZNR 12.7V 5% DO-7 PD=.4W TC=+.061%	04713	SZ10939-212
A1CR2	1901-0033	1	DIODE-GEN PRP 180V 200MA	28480	1901-0033
A1DS1	1990-0404	2	LED-VISIBLE	28480	1990-0404
A1DS2	1990-0404		LED-VISIBLE	28480	1990-0404
A1J1	1251-3283	1	CONNECTOR; 24-CONT; FEM; MICRORIBBON	28480	1251-3283
A1Q1	1854-0071	16	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q2	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q3	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q4	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q5	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q6	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q7	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q8	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q9	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q10	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q11	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q12	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q13	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q14	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q15	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q16	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1R1	0683-3025	1	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A1R2	0683-1045	3	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R3	0683-1035	3	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R4	1810-0125	2	NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0125
A1R5	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R6	1810-0125		NETWORK-RES 8-PIN SIP .125-PIN-SPCG	28480	1810-0125
A1R7	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R8	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R9	1810-0055	1	NETWORK-RES 9-PIN SIP .15-PIN-SPCG	28480	1810-0055
A1R10	0683-4725	4	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R11	0683-7525	1	RESISTOR 7.5K 5% .25W FC TC=-400/+700	01121	CB7525
A1R12	0683-8225	11	RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R13	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R14	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R15	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R16	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R17	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R18	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R19	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R20	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R21	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R22	0683-8225		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1R23	1810-0136	2	NETWORK-RES 10-PIN SIP .1-PIN-SPCG	28480	1810-0136
A1R24	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R25	1810-0136		NETWORK-RES 10-PIN SIP .1-PIN-SPCG	28480	1810-0136
A1R26	1810-0176	1	NETWORK-RES 5-PIN SIP .15-PIN-SPCG	28480	1810-0176
A1R27	0757-0123	1	RESISTOR 34.8K 1% .125W F TC=0+-100	24546	C5-1/4-TO-3482-F
A1R28	0757-0948	1	RESISTOR 10K 2% .125W F TC=0+-100	24546	C4-1/8-TO-1002-G
A1R29	0683-1335	1	RESISTOR 13K 5% .25W FC TC=-400/+800	01121	CB1335
A1R30	0683-1235	1	RESISTOR 12K 5% .25W FC TC=-400/+800	01121	CB1235
A1R31	0683-2025	2	RESISTOR 2K 5% .25W FC TC=-400/+700	01121	CB2025
A1R32	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R33	0683-5625	2	RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A1R34	0683-2025		RESISTOR 2K 5% .25W FC TC=-400/+700	01121	CB2025

Table 9L-6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R35	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A1R36	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R37	0683-4325	1	RESISTOR 4.3K 5% .25W FC TC=-400/+700	01121	CB4325
A1R38	0683-3335	1	RESISTOR 33K 5% .25W FC TC=-400/+800	01121	CB3335
A1R39	0683-3935	1	RESISTOR 39K 5% .25W FC TC=-400/+800	01121	CB3935
A1R40	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R41	0757-0444	1	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1212-F
A1S1	3101-1797	1	SWITCH ASSY, ROCKER DIP 8-SPST SW. PKG.	00779	435166-5
A1U1	1820-0939	3	IC CD4013AE	02735	CD4013AE
A1U2	1820-0583	2	IC DM74L 00N	27014	DM74L00N
A1U3	1820-0594	2	IC DM74L 72N	27014	DM74L72N
A1U4	1820-0594		IC DM74L 72N	27014	DM74L72N
A1U5	1820-0934	1	IC COMPARATOR	07263	93L24DC
A1U6	1820-0939		IC CD4013AE	02735	CD4013AE
A1U7	1260-0510	1	DUMMY IC PACKAGE	28480	1260-0510
A1U8	1820-0584	1	IC DM74L 02N	27014	DM74L02N
A1U9	1820-0588	1	IC DM74L 20N	27014	DM74L20N
A1U10	1820-0658	3	IC MULTIPLEXER	07263	93L12DC
A1U11	1818-2243	1	IC MEMORY	28480	1818-2243
A1U12	1820-0958	1	IC CD4042AE	02735	CD4042AE
A1U13	1820-0658		IC MULTIPLEXER	07263	93L12DC
A1U14	1820-1057	2	IC DM86L 76N	27014	DM86L76N
A1U15	1820-1057		IC DM86L 76N	27014	DM86L76N
A1U16	1820-0656	1	IC SN74L 98 N	01295	SN74L98N
A1U17	1820-0946	4	IC CD4001AE	02735	CD4001AE
A1U18	1820-0658		IC MULTIPLEXER	07263	93L12DC
A1U19	1820-1336	1	IC GATE	28480	1820-1336
A1U20	1820-0946		IC CD4001AE	02735	CD4001AE
A1U21	1820-0946		IC CD4001AE	02735	CD4001AE
A1U22	1820-0944	1	IC CD4025AE	02735	CD4025AE
A1U23	1820-1241	1	IC MC14512CP	04713	MC14512CP
A1U24	1820-0943	1	IC CD4023AE	02735	CD4023AE
A1U25	1820-0946		IC CD4001AE	02735	CD4001AE
A1U26	1820-0583		IC DM74L 00N	27014	DM74L00N
A1U27	1820-0586	1	IC DM74L 04N	27014	DM74L04N
A1U28	1820-0939		IC CD4013AE	02735	CD4013AE
			A1 MISCELLANEOUS		
	0380-0513	2	STANDOFF: HEX HD; 6-32 THD; 0.595 LG; 6	28480	0380-0513
	1200-0487	1		28480	1200-0487
	1530-1098	2	FASTENER:0.136" DIA 6-32 THREAD	00000	OBD
	2190-0034	2	WASHER-LK HLCL NO. 10 .194 IN ID .337 IN	28480	2190-0034
A2	05312-60002	1	INTERCONNECTION BOARD ASSEMBLY	28480	05312-60002
A2P1	1251-0099	1	CONNECTOR, 50-CONT, MALE, MICRO RIBBON	71785	57-10500-375
A2P2	1251-0101	1	CONNECTOR, 50-CONT, FEM, MICRO RIBBON	71785	57-20500-375
			CHASSIS PARTS		
	1440-0096	2	HANDLE, PLSTC W/STL INSR 8 L	12136	7835-Y12561
	1460-1312	2	SPRING LEAF BE CU	28480	1460-1312
	5040-6000	1	CATCH-SLIDE L.H.	28480	5040-6000
	5040-7001	1	CATCH-SLIDE R.H.	28480	5040-7001
	05310-20004	2	FRAME, SIDE	28480	05310-20004
	05310-40001	4	GUIDE-DOUBLE SLIDE	28480	05310-40001
	05311-00003	1	BRACKET, LEFT	28480	05311-00003
	05311-00004	1	BRACKET, RIGHT	28480	05311-00004
	05311-00005	1	SHIELD	28480	05311-00005
	05312-00001	1	PANEL, FRONT	28480	05312-00001
	05312-00002	1	PANEL, REAR	28480	05312-00002

See introduction to this section for ordering information

Table 9L-6-2. Manufacturers Code List

MFR NO.	MANUFACTURER NAME ADDRESS ZIP CODE
00779	AMP Inc., Harrisburg, Pa. 17105
01121	Allen Bradley Co., Milwaukee, Wi. 53212
01295	Texas Instrument Inc., Semiconductor Component Div., Dallas, Tx. 75231
02735	RCA Corp., Solid State Div., Sommerville, N.J. 08876
04713	Motorola Semiconductor Products, Phoenix, Az. 85008
07263	Fairchild Semiconductor Div., Mountain View, Ca. 94040
12136	Philadelphia Handle Co., Inc., Camden, N.J. 08103
24546	Corning Glass Works (Bradford), Bradford, Pa. 16701
28480	Hewlett-Packard Co., Corporate Hq., Palo Alto, Ca. 94304
71785	TRW Elek Components Cinch Div., Elk Grove Village, Il. 60007
72136	Electro Motive Mfg. Co., Inc., Willimantic, Ct. 06226

SECTION IX L
5312A ASCII INTERFACE

SUBSECTION VIII
CIRCUIT DIAGRAMS

9L-8-1. INTRODUCTION

9L-8-2. This subsection of the manual contains the following information:

a. A signal list that gives the signal name and connector pin number of each signal that interconnects the 5312A with the mainframe (see Table 9L-8-1). Other signal names used in the 5312A are defined in paragraphs 9L-4-26 and 9L-4-33.

b. Component location view of the interface assembly printed-circuit board.

c. Schematic diagram of the interface assembly.

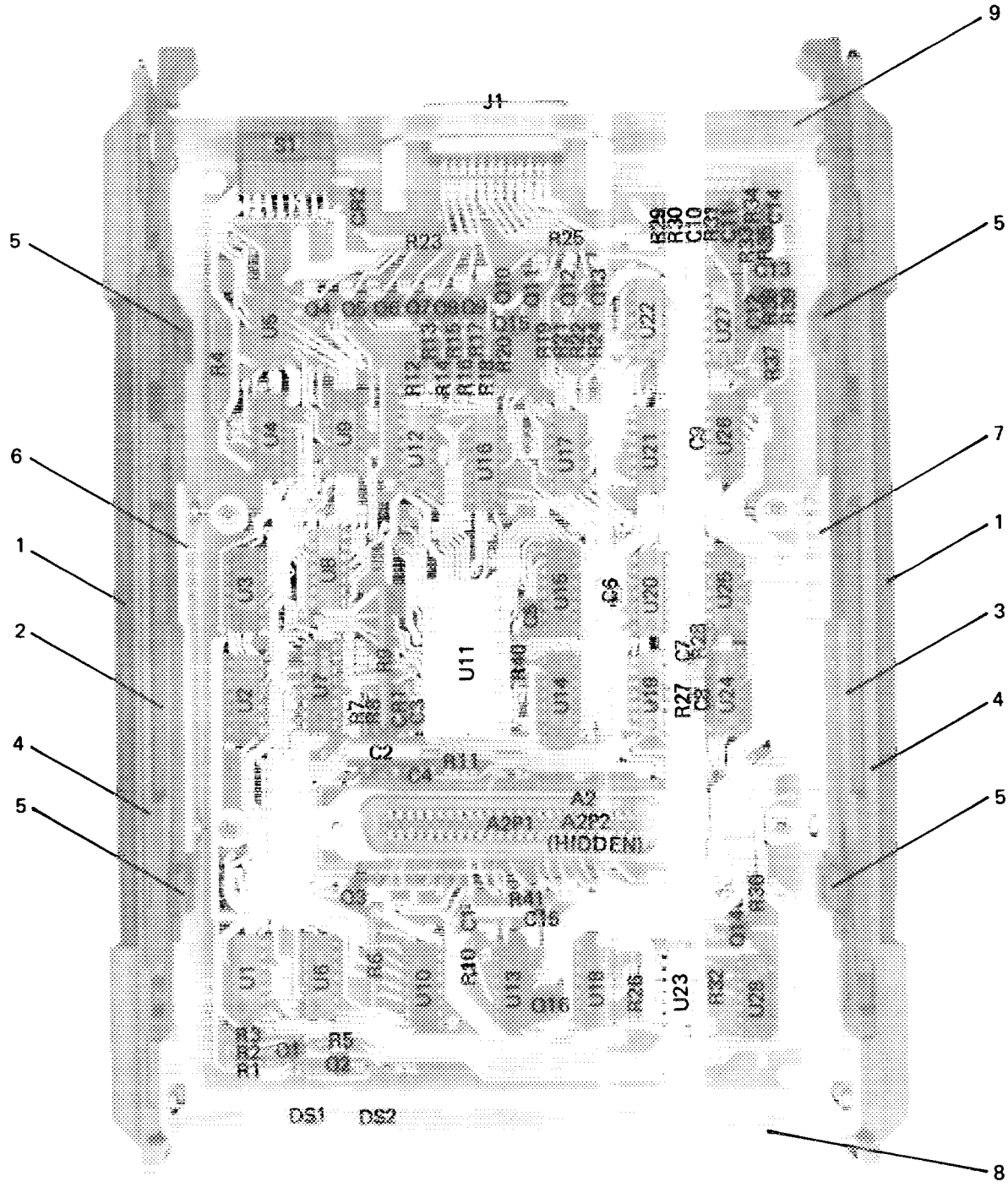
d. ASM program operational flowchart.

9L-8-3. Use the information in this subsection in conjunction with the information provided in Subsection V, Maintenance, while troubleshooting the counter.

Table 9L-8-1. Signal Interconnection List

P1 PIN NO.	SIGNAL NAME	DESCRIPTION
1 2	+5V -5V	Circuit operating voltages from the 5300B.
4	COMMON RETURN	Common power and signal return line.
8	$\overline{\text{INHIBIT}}$	High during the measurement cycle, low during the display cycle.
14	$\overline{\text{OVERFLOW}}$	Low signal enables overflow.
19	$\overline{\text{HOLD}}$	Inhibits mainframe from starting any new measurements (holds display data).
25 26	+22V +17V	Circuit operating voltages from the 5300B.
27 28 29 30 31	Hz M S K μ	Pins 27 through 31 provide the drive to the annunciator lights on the 5300B front panel. A low signal lights the corresponding indicator.
32	$\overline{\text{MANUAL RESET}}$	Low signal from mainframe front panel pushbutton switch or from 5312A clears the system to zero.
33	$\overline{\text{DP1}}$	Low signal activates decimal point 1.
34	$\overline{\text{DP2}}$	Low signal activates decimal point 2.
35	RIGHT/LEFT	Timing signal from mainframe clocks the high-speed decade latch.
36 38 40	DATA ADDRESS X DATA ADDRESS Y DATA ADDRESS Z	Digit address code X, Y, Z from the display scanner indicates a digit being displayed.
42 43 44 45	DATA D DATA C DATA B DATA A	The data code A, B, C, D represents the digit to be displayed in binary coded decimal form. Data lines are qualifiers and also may be selected by the LSB latch (U16) as the lower four bits of the ASCII character output to the bus. See paragraph 9L-4-36.
46	$\overline{\text{DP3}}$	Low signal activates decimal point 3.
47	$\overline{\text{DP4}}$	Low signal activates decimal point 4.
48	$\overline{\text{DP5}}$	Low signal activates decimal point 5.

NOTE: Pin numbers that are not listed are not connected (50-pin connector).



CABINET PARTS

ITEM	HP PART NO.	QTY	DESCRIPTION
1	1440-0096	2	HANDLE, STRAP
2	5040-6000	1	CATCH, SLIDE L.H.
3	5040-7001	1	CATCH, SLIDE R.H.
4	05310-20004	2	FRAME, SIDE
5	05310-40001	4	GUIDE, DOUBLE SLIDE
6	05311-00003	1	BRACKET, LEFT
7	05311-00004	1	BRACKET, RIGHT
8	05312-00001	1	PANEL, FRONT
9	05312-00002	1	PANEL, REAR

HEWLETT PACKARD

MANUAL CHANGES

MANUAL DESCRIPTION

INSTRUMENT: 5312A HP-IB Interface Operating & Service Manual
SERIAL PREFIX: 1428A, 1436A

DATE PRINTED: SEPT. 1975
HP PART NO: 05312-90004
MICROFICHE NO: 05312-90005

CHANGE DATE February 26, 1979

(This change supersedes all earlier dated changes)

- Make all changes listed as ERRATA.
- Check the following table for your instrument's serial prefix or serial number and make listed change(s) to manual.

IF YOUR INSTRUMENT HAS SERIAL PREFIX OR SERIAL NUMBER	MAKE THE FOLLOWING CHANGES TO YOUR MANUAL	IF YOUR INSTRUMENT HAS SERIAL PREFIX OR SERIAL NUMBER	MAKE THE FOLLOWING CHANGES TO YOUR MANUAL
1600A	1		

►**NEW OR REVISED ITEM**

►The following Service Notes are available from your local HP Sales and Service Office.

Model	Description
► 5312A-1A	Troubleshooting Procedure
► 5312A-2	Operation Verification Using 9825A Controller (All Serials)
► 5312A-3	Troubleshooting the 5312A Using Signature Analysis

ERRATA

► Page 9L-3-1, Paragraph 9L-3-6, Types of Operation:

Add the following sentence ahead of the last sentence in paragraph 9L-3-6: "The 5301A 10 MHz Counter is a TALK ONLY instrument and the 5312A ADDRESSABLE-TALK ONLY switch must always be at TALK-ONLY when the 5312A is used with a 5301A.

Change "ASCII" to "HP-IB" on front pages and any other pages where ASCII appears in the manual. This change also applies to the front-panel marking.

Page 9L-5-4, Paragraph 9L-5-22, PROCEDURES:

Replace all procedures on page 9L-5-4 with the following procedures:

9L-5-22. PROCEDURES. There are two Diagnostic Test Cards and an Interface Card that provide self check operations for use in troubleshooting. Method A uses Test 7 on Test Card B as the primary method for troubleshooting. Alternate Method B uses Test 4 on Test Card A.

The procedures are as follows:

NOTE

When using Test 7 of Test Card B, the right-most digit of the 5300B display must be a stable zero. This may be difficult to accomplish with the inherent ± 1 count variation. If this problem occurs, use Method B. If Test Cards are not available, an alternate method may be used as described in Section V Paragraph 5-48 of the manual for the 5300B mainframe. A 50-pin female connector is used in place of the test cards and wired per Table 5-2, Test 4.

2-5823-6165-6630-6986

ERRATA (Cont'd)

Method A (Test Card B, Test 7)

a. With power off, connect the 5312A to a 5300B without a plug-on module installed.

b. Remove shield plate and connect a 10528A Logic Clip to STATE ADDRESS TEST IC (U7) on the 5312A.

c. Disconnect the HP-IB cable if connected to the 5312A.

d. Insert Diagnostic Test Card "B" through Interface Card, HP Part No. 05300-60004, to 5312A 50-pin connector A2P1. Insert side of Diagnostic Card marked "TEST 7" into the Interface Card.

e. Set switches on 5312A rear panel to the following positions:

(1) Press all address switches (A1-A5) to "0" (bottom pressed in).

(2) Press TALK ONLY/ADDRESSABLE switch to ADDRESSABLE position.

(3) SHIELD switch in either position.

(4) Press SELF CHECK switch to NORM position.

(5) Turn 5300B power on.

NOTE

The SELF CHECK will not operate properly unless the right-most digit on the display is a zero.

(6) Press SELF CHECK switch to SELF CHECK position.

f. Correct operation of the 5312A is indicated as follows:

(1) The 5300B display is illuminated with an 8 in each digit position, decimals in the 5 right-most positions and overflow.

(2) The TALK indicator is illuminated.

g. If indications are incorrect (5300B display remains at 10 MHz) observe the logic states shown on the Logic Clip to determine where the program stopped (shown in the flowchart, Figure 9L-8-2, Sheet 3).

NOTE

Pins 1 through 8 of test IC (U7) show the output of State Counters U14 and U15 in binary form, which is the program line number. Convert this number to octal to locate the point in the flowchart where the program stops or loops. (Octal numbers are shown in parenthesis in the flowchart.) The logic state of the Position Counters (P1, P2, P3, and P4) is shown in the small squares adjacent to program blocks. The state of P1, P2, P3, and P4 is shown on U7 pins 12, 11, 10, and 9, respectively. The connections are shown in the schematic diagram, Figure 9L-8-1.

h. After isolating the problem area on the flowchart, refer to the schematic diagram, Figure 9L-8-1, to further isolate the problem to a component.

Method B (Test Card A, Test 4)

a. Perform test operations a through f outlined in Method A. In place of Test 7, use Diagnostic Test Card "A", Test 4.

NOTE

When this procedure is used, it is extremely important to set the SELF CHECK switch to SELF CHECK immediately after power is turned on, while the 5300B mainframe is displaying zeros. Otherwise, the unit will begin to cycle.

b. Incorrect operation is indicated when the 5300B display cycles from all 0's through all 9's. In this case, observe the logic states shown on the Logic Clip to determine where the program stopped (shown in Flowchart, Figure 9L-8-2, Sheet 3).

ERRATA (Cont'd)

Page 9L-6-4, Table 9L-6-1, Replaceable Parts:
Change A1S1 from 3101-1797 to 3101-2163, Mfr Code to 28480, and Mfr Part Number to 3101-2163.

Page 9L-8-3, Figure 9L-8-1, A1 (05312-60001) Schematic:
Change connections between A1U1, A1U6, A1U7 and A1U23 as follows:
U7(9) connected to U1A(1) and U23(4) only.
U7(10) connected to U1B(13) and U23(3) only.
U7(11) connected to U6B(13) and U23(5) only.
U7(12) connected to U6A(1) and U23(7) only.

Change P1, P2, P3, and P4 designations inside A1U7 to P4, P3, P2, and P1 respectively.

CHANGE 1 (1600A)

The two mounting studs for the HP-IB connector are changed from 0380-0513 to 0380-0644. The 0380-0644 hex studs accommodate lock screws with ISO metric thread M3.5 x 0.6 or equivalent Optimum Metric Fastener System (OMFS) thread 3.5 PO6.

Metric hardware supplied by HP for HP-IB connectors can be identified by the black finish. If metric tools are not available, a 9/32 inch hex socket will fit the 7 mm hex stud.

Conversion Kits for converting earlier instruments to use the metric lock screws are available through any HP Sales or Service Office.

CAUTION

THE THREADS OF THE METRIC HARDWARE WILL NOT FIT THE 6-32 UNC THREADS ON HARDWARE WITH A SILVER FINISH. THE THREADS WILL STRIP IF THE HARDWARE IS INTERMIXED.

Page 9L-6-3, Table 9L-6-1:

Add SERIES 1600 to A1 Description.

Change C14 (10 PF) to "Not Assigned".
Change Q15 to "Not Assigned".
Change R20 (8200Ω), R34 (2000Ω), R35 (5600Ω), and R37 (4300Ω) to "Not Assigned".

Add A1C16; 0160-2205; CAPACITOR-FXD 120 pF 5% 300WVDC MICA; 28480.

Add A1C17; 0150-0050; CAPACITOR-FXD .001 UF +80 -20% 1000 WVDC CER; 28480.

Add A1CR3; 1902-3070; DIODE-ZNR 4.22V 5% DO-7 PD = .4W TC = - .038%; 04713; SZ10939-74.

Add A1Q17; 1854-0071; TRANSISTOR-NPN SILICON PD = 300 MW FT = 200 MHz; 28480; 1854-0071.

Add A1Q18; 1854-0246; TRANSISTOR-NPN SILICON PD = 350 MW FT = 250 MHz; 04713; SPS 233.

Add A1R42; 0683-3915; RESISTOR-FXD 390 OHM 5% .25W FC TC = -400/+700; 01121; CB 3915.

Add A1R43; 0683-1225; RESISTOR-FXD 1200 OHM 5% .25W FC TC = -400/+700; 01121; CB 1225.

Add A1R44; 0683-4325; RESISTOR-FXD 4300 OHM 5% .25W FC TC = -400/+700; 01121; CB 4325.

Page 9L-8-3, Figure 9L-8-1, A1 (05312-60001) Schematic Diagram:

Change SERIES 1428A, 1436A at top of schematic to SERIES 1600.

Add capacitor C17 (.001 UF) between circuit board common and junction of U25D(13) and U20A(3) in the HOLD OFF FF circuit.

Remove connection between circuit board common and parallel-connected emitters for transistors Q4 through Q10.

Remove Q15 and 8200 ohm resistor R20 to the base of Q15. This leaves U27E(10) connected to U2D(13) only.

Remove capacitor C14 and resistors R34, R35, and R37 between U27C(6) and U27B(3).

Add C16, CR3, Q17, Q18, R42, R43, and R44 as shown in attached Figure 1.

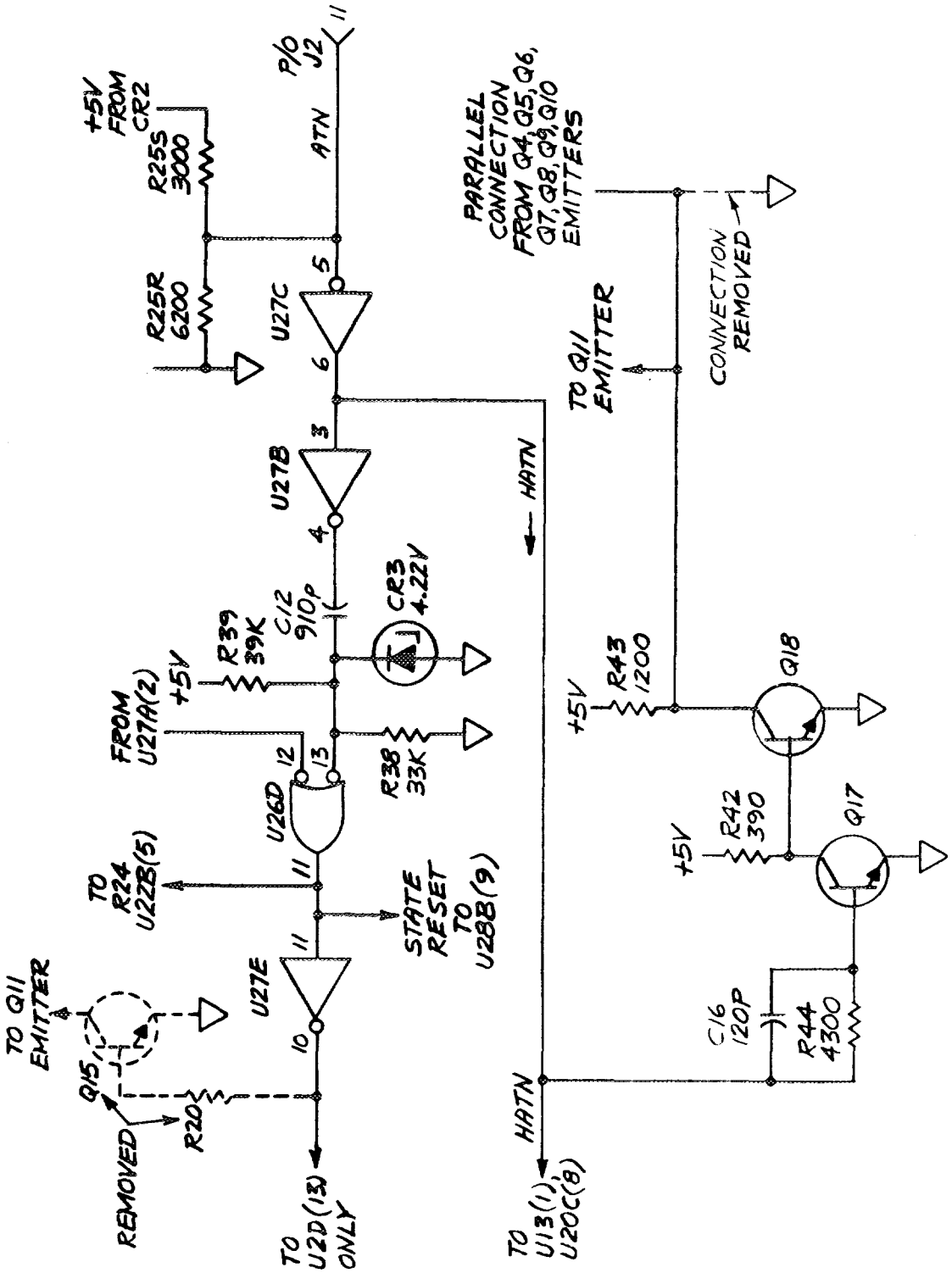


FIGURE 1. A1 CHANGES IN INTERRUPT CONTROL CIRCUIT FOR SERIES 1600